RS9113 FIPS 140-2 802.11n Module

Datasheet

Version 1.1

November 2017

Overview:

The RS9113 FIPS 140-2 Level 1 certified Wi-Fi module is based on Silicon Labs' RS9113 ultra-low-power Convergence SoC. These modules offer dual-band 1x1 802.11n. They are high performance, long range and ultra-low power modules and include a multi-threaded MAC processor called ThreadArch®, digital and analog peripheral interfaces, baseband digital signal processor, calibration OTP memory, dual-band RF transceiver, dual-band high-power amplifiers, baluns, diplexers, diversity switch and Quad-SPI flash.

The module's embedded firmware includes the WLAN protocol stack along with WPA/WPA2-PSK and WPA/WPA2-Enterprise (EAP-TLS, EAP-TTLS, EAP-PEAP) and a feature-rich TCP/IP stack thus providing a fully-integrated solution for secure embedded low-end wireless applications. These modules can be connected to 8/16/32-bit host processors through SPI, UART, USB and USB-CDC interfaces.

The modules are available in a small footprint form factor with low BoM requirement.

Applications:

- Smartphones, Tablets
- Secure VoWi-Fi phones
- Smart meters and in-home displays
- Secure Industrial automation and telemetry
- Secure Medical devices
- Industrial monitoring and control

Module Features

WLAN:

- Compliant to single-spatial steam IEEE 802.11 a/b/g/n with dual band (2.4 and 5 GHz) support.
- Support for 20MHz channel bandwidth.
- Transmit power up to +18dBm with integrated PA.
- Receive sensitivity of -97dBm.

Software/Firmware:

- WLAN stack embedded in the device.
- Supports WPA/WPA2-PSK, WPA/WPA2-Enterprise (EAP-TLS, EAP-TTLS, EAP-PEAP)
- TCP/IP stack embedded in the device – includes:
  - IPv4 and IPv6
  - DHCP Server/Client
  - HTTP Server/Client
  - Static and Dynamic Webpages with JSON Objects (for HTML Server)
  - ICMP
  - Websockets
  - DNS Client
  - IGMP
  - SNMP

FIPS:

- FIPS 140-2 Level 1 Certification.
- FIPS Approved and non-FIPS Approved modes of operation.
- FIPS Approved Algorithms
  - AES 128-bit in CBC mode Encrypt/Decrypt key wrapping
  - AES 256-bit in CBC mode Encrypt/Decrypt key wrapping
  - AES CCM
  - AES-128 CMAC
  - SHA-1, SHA-256
  - HMAC-SHA1, HMAC-SHA256
  - RSA PKCS#5 v1.5 with 2048-bit key and SHA-256 for Digital Signature Generation/Verification
  - SP800-90 DRBG HASH_DRBG
  - SP800-108 KDF
  - CVL: SP800-135 TLS v1.0 KDF
- Non-approved Algorithms allowed in FIPS mode
  - Hardware non-deterministic random number generator
  - Diffie Hellman
  - RSA
- Non-approved Algorithms for non-FIPS mode
  - RC4
  - DES
  - MD4
  - MD5
- Support for Power-up tests like Cryptographic Algorithm tests, Firmware/Bootloader integrity tests, Critical functions tests
- Support for Conditional tests like Firmware load test, Manual key entry test and Continuous random number generator test

General:

- FCC, IC, ETSI/CE Certified
- SPI, UART, USB, USB-CDC host interfaces.
- Wireless firmware upgrade.
- Options for Single supply of 3.0 to 3.6 V operation or multiple supplies for power saving[1].
- Operating temperature range: -40°C to +85°C

[1] USB Interface needs VBUS level of 5V for detection and enumeration.

About this Document

This document describes the RS9113 FIPS 140-2 Level 1 certified 802.11n modules. The document covers the modules' hardware and software features, package descriptions, pin descriptions, interface specifications, electrical characteristics, performance specifications, reliability and certification information and ordering information.

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1 Overview

The RS9113 FIPS 140-2 Level 1 certified Wi-Fi module is based on Silicon Labs' RS9113 ultra-low-power Convergence SoC. These modules offer dual-band 1x1 802.11n. They are high performance, long range and ultra-low power modules and include a multi-threaded MAC processor called ThreadArch®, digital and analog peripheral interfaces, baseband digital signal processor, calibration OTP memory, dual-band RF transceiver, dual-band high-power amplifiers, baluns, diplexers, diversity switch and Quad-SPI flash.

The module's embedded firmware includes the WLAN protocol stack along with WPA/WPA2-PSK and WPA/WPA2-Enterprise (EAP-TLS, EAP-TTLS, EAP-PEAP) and a feature-rich TCP/IP stack thus providing a fully-integrated solution for secure embedded low-end wireless applications. These modules can be connected to 8/16/32-bit host processors through SPI, UART, USB and USB-CDC interfaces.

The modules are available in a small footprint form factor with low BoM requirement.

1.1 Block Diagram

The following figure is the block diagram for the FIPS 140-2 Level 1 Certified module.

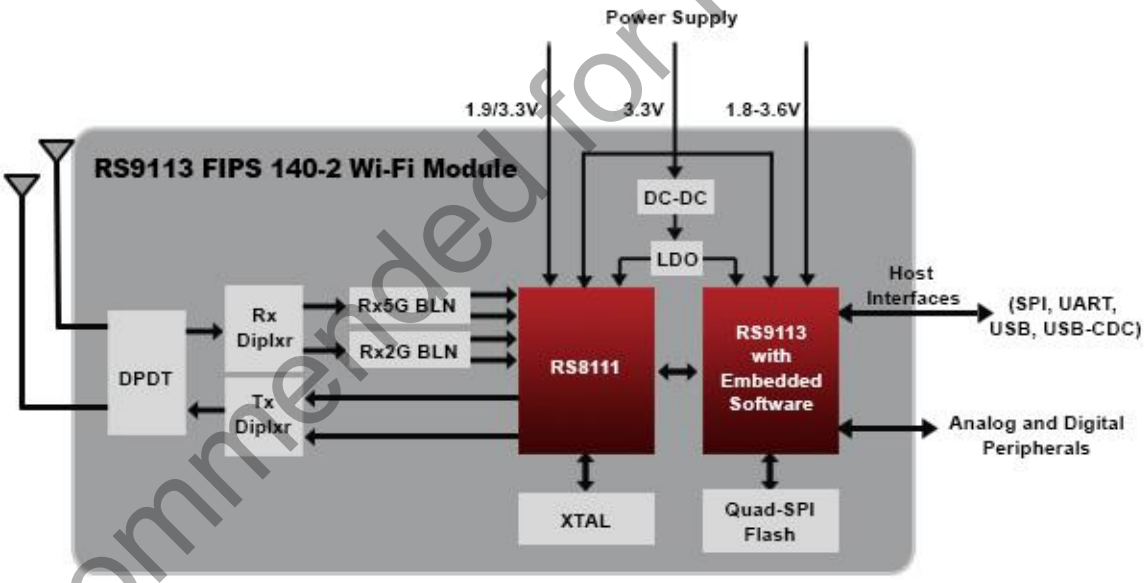


Figure 1: Block Diagram of RS9113 FIPS 140-2 Certified Module

1.2 Part Numbering and Variants

The FIPS 140-2 Level 1 Certified Wi-Fi Module is presently available as two variants – 1x1 802.11n Dual Band (2.4 GHz and 5 GHz) with and without integrated Antenna. The part numbers for these modules are RS9113-N00-D0F and RS9113-N00-D1F[2] respectively.

Silicon Labs offers multiple other variants which are not FIPS Certified. These variants are listed below. Contact Silicon Labs Sales for details on how to get FIPS 140-2 Level 1 Certification for these variants.

[2] Contact Redpine for the certification status.

1) Single Band (2.4 GHz) without Antenna
2) Single Band (2.4 GHz) with Antenna

Apart from the hardware variants listed above, the module can also be offered with the following features included.

1) FTP Client
2) SNTP
3) mDNS Client
4) DNS-SD Client
5) SSL 3.0/TSL 1.2
6) HTTPS Server/Client

2 Features

The table below lists the features supported by the RS9113 FIPS 140-2 Level 1 Certified module.

S.No.	Feature	Description
1.	Wireless Protocols	IEEE 802.11a, 802.11b, 802.11g, 802.11n
2.	Operational Modes Supported	Wi-Fi Client in FIPS and non-FIPS modes
3.	WLAN Data Rates	802.11b: 1, 2, 5.5, 11 Mbps 802.11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps 802.11n: MCS0 to MCS7 with and without Short GI
4.	WLAN Bandwidth	20 MHz
5.	WLAN Operating Frequency Range	2412 MHz – 2484 MHz 4910 MHz – 5825 MHz
6.	WLAN Modulation	OFDM with BPSK, QPSK, 16-QAM, and 64-QAM 802.11b with CCK and DSSS
7.	WLAN Transmit Power	18 dBm
8.	WLAN Receive Sensitivity	-97 dBm
9.	WLAN Features	Dynamic selection of data rate depending on the channel statistics. Hardware accelerators for WEP 64/128-bit, TKIP, AES and WPS Support for WMM Support for AMPDU Aggregation/De-aggregation and AMSDU De-aggregation Support for IEEE 802.11d/e/i
10.	TCP/IP Features	IPv4 and IPv6 DHCP Server/Client HTTP Server/Client Static and Dynamic Webpages with JSON Objects (for HTML Server) ICMP Websockets DNS Client IGMP SNMP

S.No.	Feature	Description
11.	Deep Sleep Current Consumption	< 10 µA in disconnected state < 30 µA in connected state
12.	Host Interfaces	SPI UART USB 2.0/1.1 USB-CDC
13.	USB Host Interface	Supports 480 Mbps High Speed (HS) mode and 12 Mbps Full Speed (FS) modes.
14.	SPI Host Interface	Maximum clock speed of 80MHz Support for SPI Modes 0 (CPOL=0, CPHA=0) and 3 (CPOL=1, CPHA=1)
15.	UART Host Interface	Supported Baud Rates (bps): 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600 Support for AT and Binary Commands for Configuration and Data Transfer Support for 8 bits encoding Support for 1 stop bit Support for Auto Flow Control Support for Transparent Mode
16.	Wireless Security Features	WPA/WPA2-Personal WPA/WPA2 Enterprise: EAP-TLS EAP-TTLS EAP-PEAP WPS (embedded in the device)
17.	Application throughputs[3]	With embedded TCP/IP Stack: Upto 25 Mbps UDP Upto 20 Mbps TCP

[3] The throughputs mentioned here have been recorded in an ideal environment on an x86 platform over USB. Throughputs observed in other environments might differ based on the host interface speeds (e.g., SPI clock frequency, UART Baud Rate, etc.), host processor capabilities (CPU frequency, RAM, etc.), wireless medium, physical obstacles, distance, etc.

S.No.	Feature	Description
		With TCP/IP Stack in Host: Upto 40 Mbps UDP Upto 25 Mbps TCP
18.	FIPS Security Level Specification	Cryptographic Module Specification: Level 1 Cryptographic Module Ports and Interfaces: Level 1 Roles, Services, and Authentication: Level 1 Finite State Model: Level 1 Physical Security: Level 1 Operational Environment: N/A Cryptographic Key Management: Level 1 EMI/EMC: Level 1 Self-tests: Level 1 Design Assurance: Level 1 Mitigation of Other Attacks: N/A
19.	FIPS Roles Supported	Cryptographic Officer Role User Role
20.	FIPS Approved Algorithms	AES with 128-bit key and 256-bit key in CBC mode Encrypt/Decrypt, key wrapping (Cert. #3299) AES CCM (Cert. #3300) AES-128 CMAC (Cert. #3316) SHA-1, 256 (Cert. #2628) HMAC-SHA1 and HMAC-SHA256 (Cert. #2003) RSA PKCS#5 v1.5 with 2048-bit key and SHA-256 for Digital Signature Generation/Verification (Cert. #1689) SP800-90 DRBG HASH_DRBG (Cert. #754) SP800-108 KDF (Cert. #50) CVL: SP800-135 TLS v1.0 KDF (Cert. #474)
21.	Non-approved Algorithms allowed in FIPS mode	Hardware non-deterministic random number generator (for seeding Approved DRBG) Diffie-Hellman (key agreement; key establishment methodology provides 112 bits of encryption strength) RSA (key wrapping; key establishment methodology provides 112 bits of encryption strength)

S.No.	Feature	Description
22.	Non-approved Algorithms, allowed only in non-FIPS mode	RC4 DES MD4 MD5
23.	Power-up Self Tests in FIPS mode	Cryptographic Algorithm Tests: SHA1 KAT SHA256 KAT HMAC-SHA1 KAT HMAC-SHA256 KAT RSA 2048 Signature Generation KAT RSA 2048 Signature Verification KAT AES-128 CBC Encrypt KAT AES-128 CBC Decrypt KAT AES-256 CBC Encrypt KAT AES-256 CBC Decrypt KAT SP800-38F AES Key Wrap Encrypt KAT SP800-38F AES Key Wrap Decrypt KAT SP800-90 DRBG KAT SP800-135 TLS KDF KAT SP800-108 KDF KAT AES-CCM KAT Software/Firmware Tests: Firmware integrity test (32-bit checksum) Boot-loader integrity test (32-bit checksum) Critical Functions Tests: SHA1 checksum of configuration parameters
24.	Conditional Tests in FIPS mode	Firmware load test: AES CMAC Test Manual key entry test: 256-bit PSK Continuous random number generator tests Continuous test on SP800-90 DRBG Continuous test on non-Approved NDRNG

S.No.	Feature	Description
25.	Critical Security Parameters (CSPs) contained in the module	SP800-90 DRBG Seed Material SP800-90 DRBG Internal State WPA2 Pre-shared Key 802.11i KDF Internal State 128-bit AES-CCM keys used as 802.11i Temporal keys HMAC-SHA1 key for 802.11i MIC keys 802.11i Key Encryption Key used for relaying GTK from AP 802.11i Group Temporal Key (GTK) EAP-TLS Encryption Key EAP-TLS Integrity Key EAP-TLS Peer Encryption Key RSA KDK 2048-bit private key of client certificate RADIUS server password EAP-TTLS Master Secret Key EAP-TTLS Master Session Key EAP-TTLS Extended Master Session Key EAP-TTLS PRF seed material EAP-TTLS Integrity Key EAP-PEAP Master Session Key EAP-PEAP Extended Master Session Key EAP-PEAP Compound Session Key EAP-PEAP PRF seed material EAP-PEAP Integrity Key
26.	Public Keys contained in the module	Client EAP-TLS RSA Public Key used in the client certificate Server EAP-TLS RSA Public Key used in the server certificate CA certificate RSA Public Key Server EAP-TTLS RSA Public Key Server EAP-PEAP RSA Public Key
27.	Operating Temperature Range	-40°C to +85°C
28.	Supply Voltages and Options[4]	Option 1: Single 3.0 to 3.6V Supply

[4] USB Interface needs VBUS level of 5V for detection and enumeration.

S.No.	Feature	Description
		Option 2[5]: A 3.0 to 3.6V Supply, a 1.8 to 3.6V Supply and a 1.9 to 3.6V Supply
29.	Power Save Modes[6]	Dynamic Clock Gating Low Power (LP) Mode – Modem and RF Transceiver Powered off. Host Interface is active. Supported with all host interfaces. Ultra Low Power (ULP) Mode – Most of the module powered off except for a small portion running a timer. Host interface is inactive. Entry and exit of sleep mode can be through packet or GPIO based handshake. Supported only in SPI, UART modes.
30.	Miscellaneous Features	Wireless Firmware Upgrade Wireless Configuration

Table 1: RS9113 FIPS 140-2 Certified Module Features

[5] This option results in lower power consumption overall. Refer to the Module Integration Guide for details on the circuit.
[6] Refer to Programmer Reference Manual/API User Guide for more details on how to use these modes. Refer to the GPIO section of the Pin Description table to understand the signal requirements for these modes.

3 Package Description

The RS9113 FIPS Module is offered in a small footprint form factor with low BoM requirement.

3.1 Package Description of Module Without Antenna

3.1.1 Mechanical Characteristics

Parameter	Value (L X W X H)	Units
Module Dimensions	14 x 15 x 2.1	mm
Tolerance	±0.2	mm

Table 2: Mechanical Dimensions of the FIPS 140-2 Module Without Antenna

3.1.2 Package Dimensions

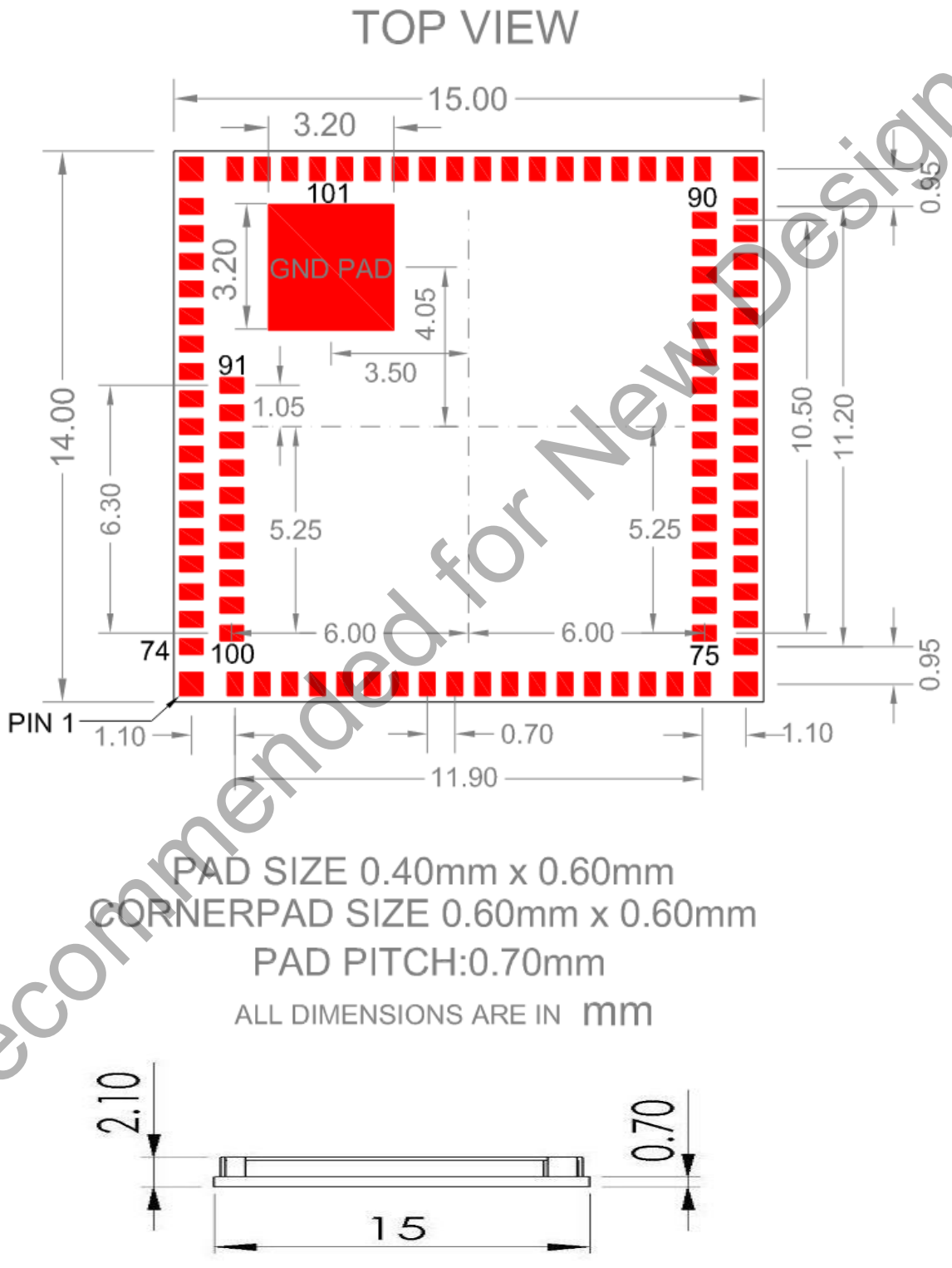


Figure 2: Package Dimensions of the FIPS 140-2 Module Without Antenna

3.1.3 PCB Landing Pattern

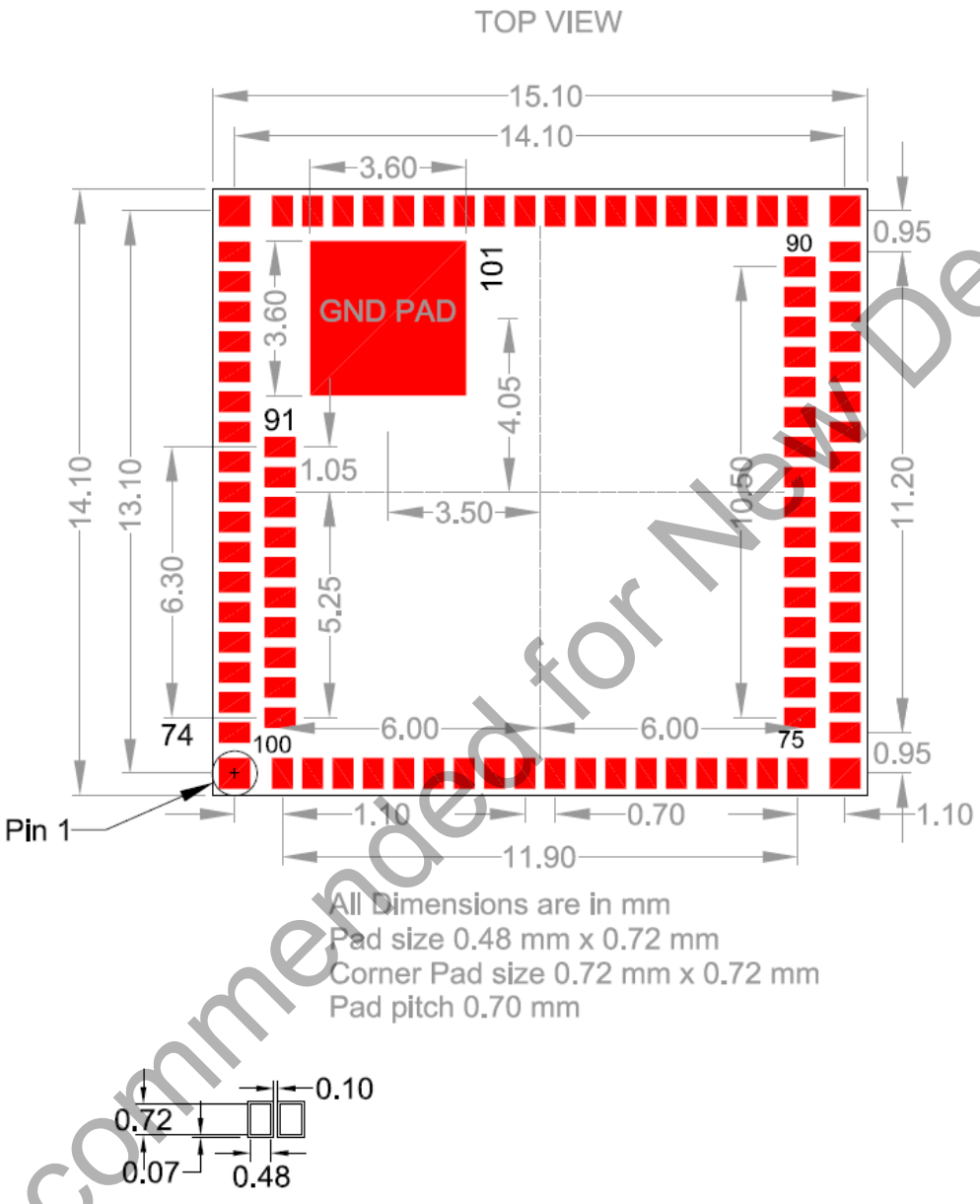


Figure 3: PCB Landing Pattern of the FIPS 140-2 Module Without Antenna

3.2 Package Description of Module With Antenna

3.2.1 Mechanical Characteristics

Parameter	Value (L X W X H)	Units
Module Dimensions	27 x 16 x 3.1	mm
Tolerance	±0.2	mm

Table 3: Mechanical Dimensions of the FIPS 140-2 Module With Antenna

3.2.2 Package Dimensions

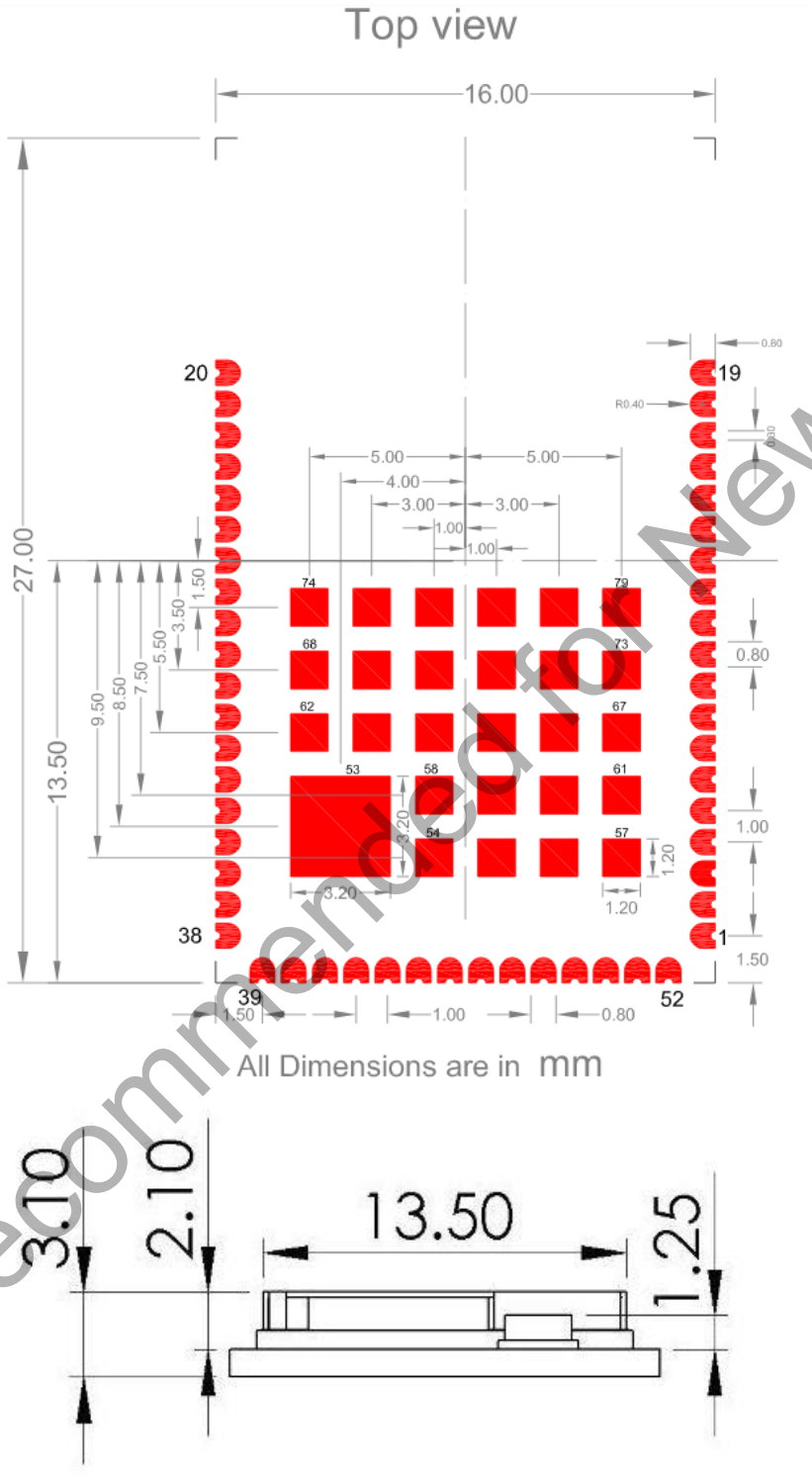


Figure 4: Package Dimensions of the FIPS 140-2 Module With Antenna

3.2.3 PCB Landing Pattern

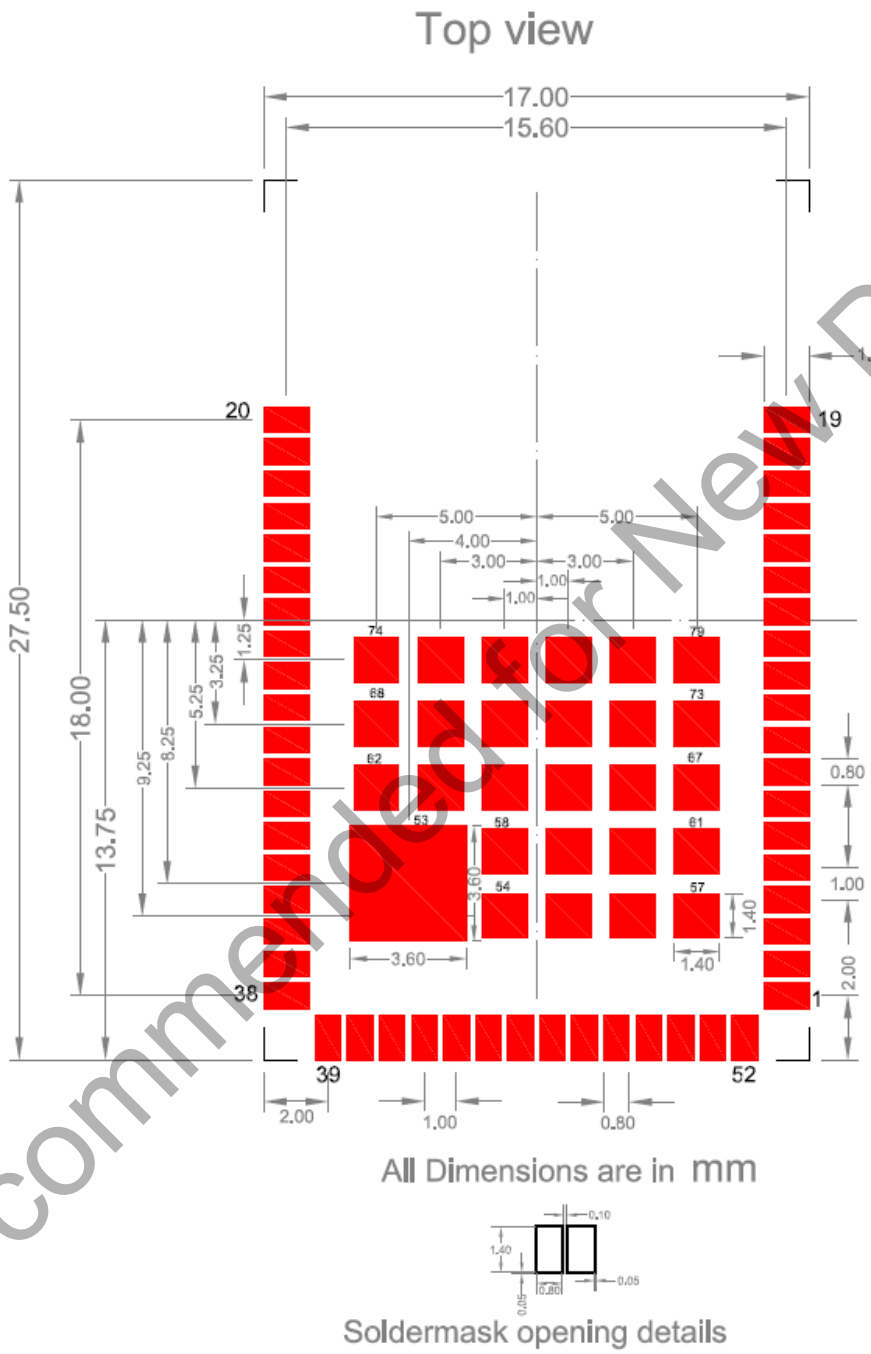


Figure 5: PCB Landing Pattern of the FIPS 140-2 Module With Antenna

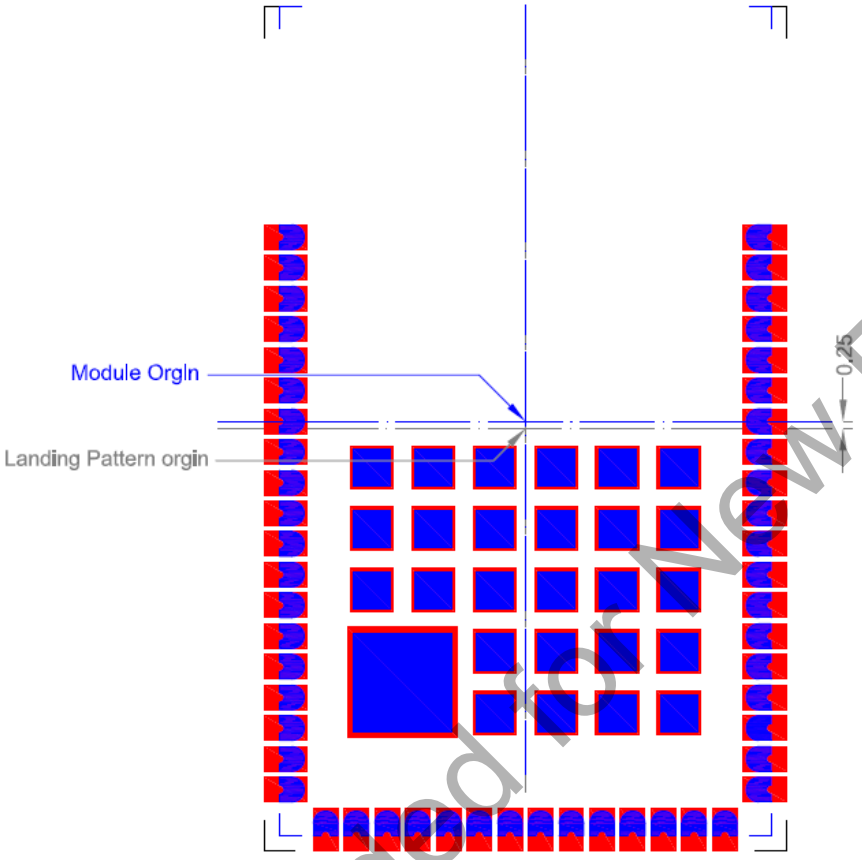


Figure 6: Mounting View of the FIPS 140-2 Module With Antenna

3.3 Recommended Reflow Profile

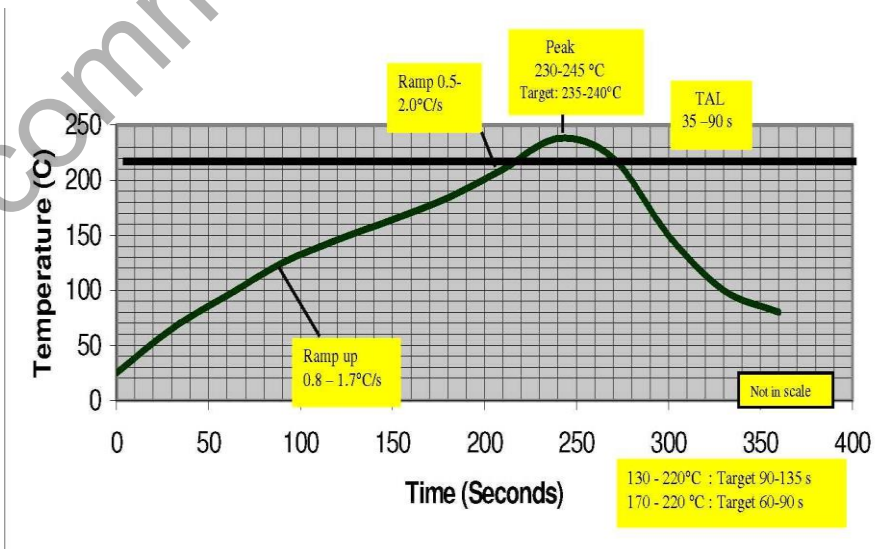


Figure 7: Reflow Diagram

Note: The profile shown is based on SAC 305 solder (3% silver, 0.5% copper). We recommend the ALPHA OM-338 lead-free solder paste. This profile is provided mainly for guidance. The total dwell time depends on the thermal mass of the assembled board and the sensitivity of the components on it. The recommended belt speed is 50-60 Cm/Min. A finished module can go through 2 more reflow processes

3.4 Baking Instructions

The RS9113 module packages are moisture sensitive and devices must be handled appropriately. After the devices are removed from their vacuum sealed packs, they should be taken through reflow for board assembly within 168 hours at room conditions, or stored at under 10% relative humidity. If these conditions are not met, the devices must be baked before reflow. The recommended baking time is nine hours at 125°C.

4 Pinout and Pin Description

4.1 Pinout of the FIPS 140-2 Module Without antenna

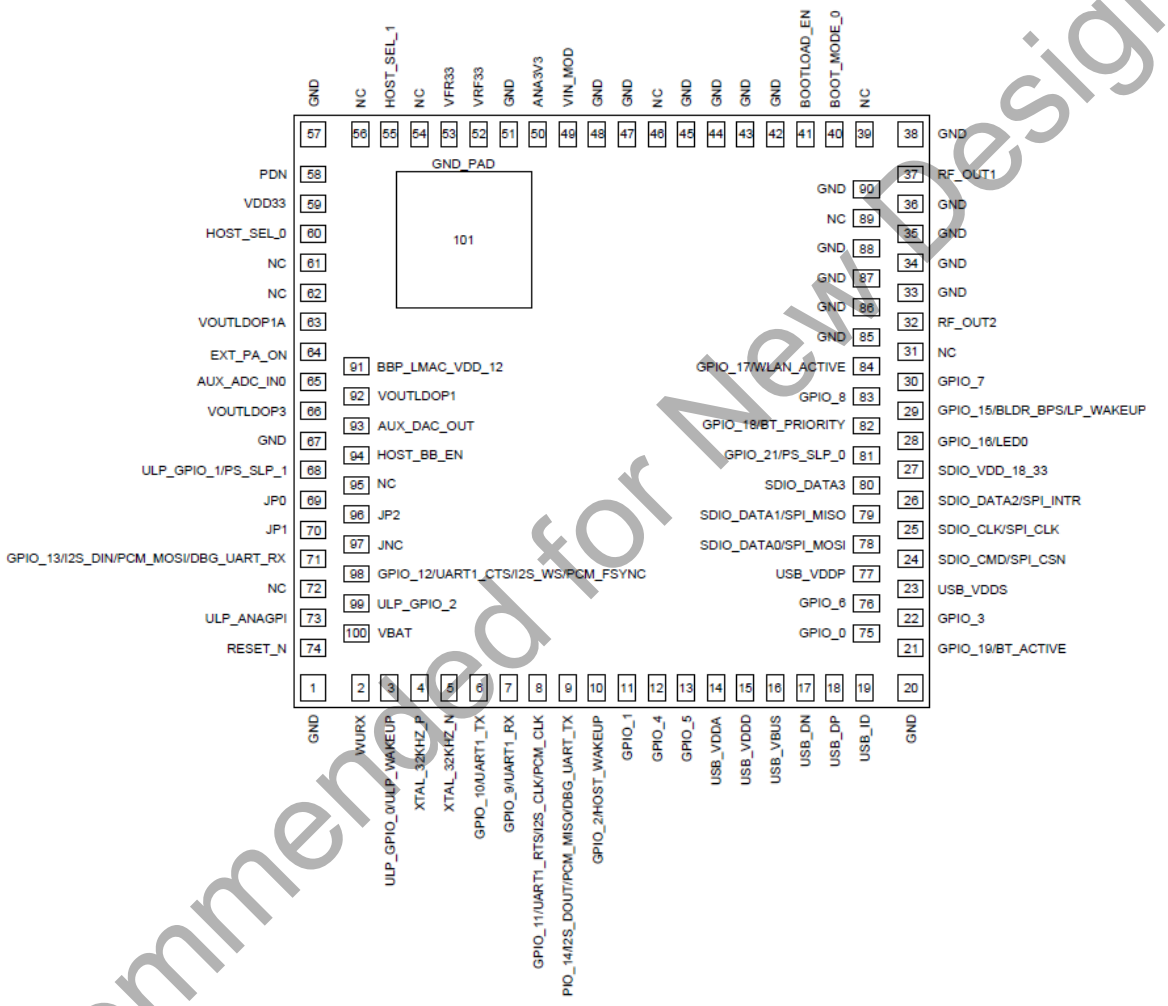


Figure 8: Pinout Diagram of the FIPS 140-2 Module Without Antenna

4.2 Pinout of the FIPS 140-2 Module With Integrated Antenna

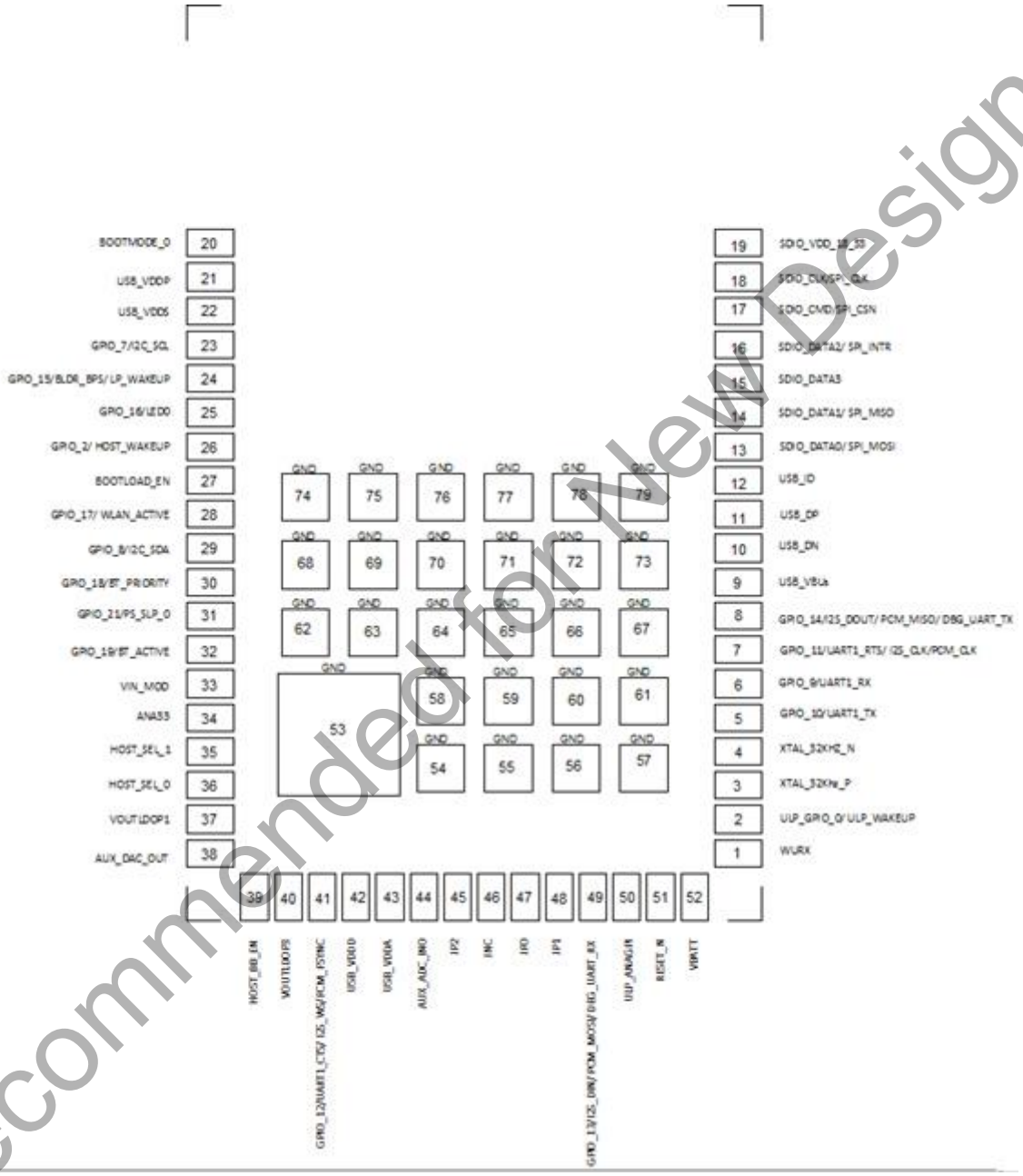


Figure 9: Pinout Diagram of the FIPS 140-2 Module with Antenna

4.3 Pin Description

This section describes the pins of the two packages of RS9113 FIPS 140-2 Module. The information contained here should be used along with the information in the Module Integration Guide.

S.No	Pin Name	Pin # in RS9113-N00-D0F	Pin # in RS9113-N00-D1F	Direction	Description
Control and RF Interface					
1.	RESET_N	74	51	Input	Active-low asynchronous reset signal. The minimum reset assertion time is 20 ms.
2.	RF_OUT_2	32	---	RF In/RF Out	Default Antenna port. Connect to Antenna with a 50 Ω impedance. Refer to Module Integration Guide for details.
3.	RF_OUT_1	37	---	RF In/RF Out	Used in the case of Antenna Diversity[7]. If used, connect to Antenna with a 50 Ω impedance and follow same guidelines as RF_OUT_2 from Module Integration Guide. If unused, leave unconnected.
Power and Ground Interface[8]					
4.	VIN_MOD	49	33	Input	3.3V Digital Power Supply
5.	ANA33	50	34	Input	1.9V to 3.6V Analog Power Supply
6.	SDIO_VDD_18_33	27	19	Input	3.3V Digital Power Supply
7.	VBATT	100	52	Input	1.8V to 3.6V Digital Power Supply.
8.	VRF33	52, 53	---	Input	3.3V Analog Supply for the RF Transceiver.
9.	VDD33	59	---	Input	3.3V Digital Supply for the RF Transceiver.
10.	VOUTLDOP1	92	37	Output	USB Mode: Connect to USB_VDDD. Other Modes: Leave unconnected.
11.	VOUTLDOP3	66	40	Output	USB Mode: Connect to USB_VDDP. Other Modes: Leave unconnected.
12.	VOUTLDOP1A	63	---	Output	Connect to BBP_LMAC_VDD_12 through a filter. Refer to the Module Integration Guide for more details.

[7]Supported in future software releases.
[8]Refer to the Module Integration Guide for recommendations on different supplies.

S.No	Pin Name	Pin # in RS9113-N00-D0F	Pin # in RS9113-N00-D1F	Direction	Description
13.	BBP_LMAC_VDD_12	91	---	Input	Connect to the VOUTLDOP1A pin through a filter. Refer to the Module Integration Guide for more details.
14.	USB_VDDA	14	43	Input	USB Mode: 3.3V Analog Supply. Other Modes: Connect to Ground.
15.	USB_VDDS	23	22	Input	USB Mode: 3.3V Digital Supply. Other Modes: Connect to Ground.
16.	USB_VDDP	77	21	Input	USB Mode: Connect to VOUTLDOP3. Other Modes: Connect to Ground.
17.	USB_VDDD	15	42	Input	USB Mode: Connect to VOUTLDOP1. Other Modes: Connect to Ground.
18.	GND	1, 20, 33, 34, 35, 36, 38, 42, 43, 44, 45, 47, 48, 51, 57, 67, 85, 86, 87, 88, 90, 101	53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79	Ground	Common Ground
SDIO, Slave SPI and USB Interfaces					
19.	SDIO_CLK/SPI_CLK	25	18	Input	SDIO & SPI Modes: Interface clock from Host processor
				Input	Other modes: Reserved. Connect to Ground.
20.	SDIO_CMD/SPI_CSN	24	17	Inout	SDIO Mode: SDIO Interface Command Signal
				Input	SPI Mode: Active-low SPI Chip Select Signal
				Input	Other Modes: Reserved. Connect to Ground.
21.	SDIO_DATA0/SPI_MOSI	78	13	Inout	SDIO Mode: SDIO Interface Data0 Signal

S.No	Pin Name	Pin # in RS9113-N00-D0F	Pin # in RS9113-N00-D1F	Direction	Description
				Input	SPI Mode: SPI Master-Out-Slave-In Signal
				Output	Other Modes: Reserved. Leave unconnected.
22.	SDIO_DATA1/SPI_MISO	79	14	Inout	SDIO Mode: SDIO Interface DATA1 Signal
				Output	SPI Mode: SPI Master-In-Slave-Out Signal
				Input	Other Modes: Reserved. Connect to Ground.
23.	SDIO_DATA2/SPI_INTR	26	16	Inout	SDIO Mode: SDIO Interface DATA2 Signal
				Output	SPI Mode: Interrupt Signal to the Host. Active-high level, Active-low level and Open Drain modes are supported. In ULP mode, a pull-up or pull-down resistor of 100 kΩ might be required depending on whether the signal is configured as Active-low or Active-high. The pull-up/pull-down resistor can be avoided if the Host can mask this interrupt before the module enters ULP Sleep mode and unmask it after it exits ULP Sleep mode.
				Input	Other modes: Reserved. Connect to Ground.
24.	SDIO_DATA3	80	15	Inout	SDIO Mode: SDIO Interface DATA3 Signal
				Input	Other Modes: Reserved. Connect to Ground.
25.	USB_VBUS	16	9	Input	USB Mode: 5V VBUS Signal from USB Connector.
				Input	Other Modes: Leave unconnected.
26.	USB_DN	17	10	Inout	Negative Data Channel from USB Connector.

S.No	Pin Name	Pin # in RS9113-N00-D0F	Pin # in RS9113-N00-D1F	Direction	Description
				Inout	Other Modes: Leave unconnected.
27.	USB_DP	18	11	Inout	Positive Data Channel from USB Connector.
				Inout	Other Modes: Leave unconnected.
28.	USB_ID	19	12	Inout	ID signal from USB Connector.
				Inout	Other Modes: Leave unconnected.
GPIO Interface[9]					
29.	GPIO_0	75	---	Inout	Reserved – connect a 100 kΩ pull-down resistor.
30.	GPIO_1	11	---	Inout	Reserved – connect a 100 kΩ pull-up resistor.
31.	GPIO_2/HOST_WAKE UP	10	26	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Output	Host Wakeup Interrupt Mode: This pin is used by firmware to indicate a pending packet to the Host processor. It should be used only if the Host processor is not able to wake up from a sleep state using the host interface specific interrupt like SDIO_DATA2/SPI_INTR. A pull up or pull down has to be placed on this pin based on whether the pin is configured as active low or active high interrupt in the Host processor, respectively. This feature can be enabled and configured through API (for WiSeConnect®/Connect-io-n®) and driver settings (for n-Link®).
32.	GPIO_3	22	---	Inout	Reserved – connect a 100 kΩ pull-up resistor if ULP Sleep Mode is used and VINMOD (3.3V) is not switched off using an external load switch and HOST_BB_EN signal – refer to the Module Integration Guide for the circuit details.

[9]All unused GPIOs can be configured by the Host processor (through a software command) as outputs to reduce current consumption.

S.No	Pin Name	Pin # in RS9113-N00-D0F	Pin # in RS9113-N00-D1F	Direction	Description
33.	GPIO_4	12	---	Inout	Reserved – connect a 100 kΩ pull-up resistor if ULP Sleep Mode is used and VINMOD (3.3V) is not switched off using an external load switch and HOST_BB_EN signal – refer to the Module Integration Guide for the circuit details.
34.	GPIO_5	13	---	Inout	Reserved – connect a 100 kΩ pull-up resistor if ULP Sleep Mode is used and VINMOD (3.3V) is not switched off using an external load switch and HOST_BB_EN signal – refer to the Module Integration Guide for the circuit details.
35.	GPIO_6	76	---	Inout	Reserved – connect a 100 kΩ pull-up resistor if ULP Sleep Mode is used and VINMOD (3.3V) is not switched off using an external load switch and HOST_BB_EN signal – refer to the Module Integration Guide for the circuit details.
36.	GPIO_7/I2C_SCL	30	23	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Input	I^2C Mode: I^2C interface clock signal – connect a 10 kΩ pull-up resistor on this signal as per the I^2C standard. This feature is supported only when the I^2S mode is enabled in the n-Link™ releases v1.5.0 onwards. In WiSeConnect™ this feature is supported for IAP communication from release 1.6.0 onwards.
37.	GPIO_8/I2C_SDA	83	29	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Inout	I^2C Mode: I^2C interface data signal – connect a 10 kΩ pull-up resistor on this signal as per the I^2C standard. This feature is supported only when the I^2S mode is enabled in the n-Link™ releases v1.5.0 onwards. In WiSeConnect™ this feature is

S.No	Pin Name	Pin # in RS9113-N00-D0F	Pin # in RS9113-N00-D1F	Direction	Description
					supported for IAP communication from release 1.6.0 onwards.
38.	GPIO_9/UART1_RX	7	6	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Input	UART Mode: UART 1 Serial Input. This pin is configured as UART pin if UART is selected as the Host Interface.
39.	GPIO_10/UART1_TX	6	5	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Output	UART Mode: UART 1 Serial Output. This pin is configured as UART pin if UART is selected as the Host Interface.
40.	GPIO_11/UART1_RTS /I2S_CLK/PCM_CLK	8	7	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Output	UART Mode: UART 1 Request To Send – connect a 100 kΩ pull-down resistor if the host is not controlling this signal at all times. This pin is configured as UART pin if UART is selected as the Host Interface.
				Input	I^2S Mode: I2S Clock signal. Supported only in n-Link™ in Slave mode from release v1.5.0 onwards.
				Input	PCM Mode: PCM Clock signal. Supported only in n-Link™ in Slave mode from release v1.5.0 onwards.
41.	GPIO_12/UART1_CTS /I2S_WS/PCM_FSYNC	98	41	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Input	UART Mode: UART 1 Clear To Send – connect a 100 kΩ pull-down resistor if the host is not controlling this signal at all times. This pin is configured as UART pin if UART is selected as the Host Interface.
				Input	I^2S Mode: I2S WS signal. Supported only in n-Link™ in Slave mode from release v1.5.0 onwards.

S.No	Pin Name	Pin # in RS9113-N00-D0F	Pin # in RS9113-N00-D1F	Direction	Description
				Input	PCM Mode: PCM FSYNC signal. Supported only in n-Link™ in Slave mode from release v1.5.0 onwards.
42.	GPIO_13/I2S_DIN/PCM_MOSI/DBG_UART_RX	71	49	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Input	UART Mode: UART 2 (Debug) Serial Input.
				Input	I^2S Mode: I2S Data Input signal. Supported only in n-Link™ in Slave mode from release v1.5.0 onwards.
				Input	PCM Mode: PCM Master-Out-Slave-In signal. Supported only in n-Link™ in Slave mode from release v1.5.0 onwards.
43.	GPIO_14/I2S_DOUT/PCM_MISO/DBG_UART_TX	9	8	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Output	UART Mode: UART 2 (Debug) Serial Output.
				Output	I^2S Mode: I2S Data Output signal. Supported only in n-Link™ in Slave mode from release v1.5.0 onwards.
				Output	PCM Mode: PCM Master-In-Slave-Out signal. Supported only in n-Link™ in Slave mode from release v1.5.0 onwards.
44.	GPIO_15/BLDR_BPS/LP_WAKEUP	29	24	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Input	BLDR_BPS/LP_WAKEUP – in this mode, the signal has two functionalities – one during the bootloading process and one after the bootloading. During bootloading, this signal is an active-high input to indicate that the bootloader should bypass any inputs from the Host processor and continue to load the default firmware from Flash. After bootloading, this signal is an active-high input to indicate that the module

S.No	Pin Name	Pin # in RS9113-N00-D0F	Pin # in RS9113-N00-D1F	Direction	Description
					should wakeup from its Low Power (LP) sleep mode. The BLDR_BPS functionality is valid only for WiSeConnect®/Connect-io-n® modules.
45.	GPIO_16/LED0	28	25	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Output	LED Mode: Control signal for an external LED.
46.	GPIO_17/WLAN_ACTIVE	84	28	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Output	Bluetooth Coexistence Mode: Active-high signal to indicate to an external Bluetooth IC that WLAN transmission is active. Not supported in the current firmware.
47.	GPIO_18/BT_PRIORITY	82	30	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Input	Bluetooth Coexistence Mode: Active-high signal used to indicate to the module that Bluetooth transmissions are higher priority. Not supported in the current firmware.
48.	GPIO_19/BT_ACTIVE	21	32	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Input	Bluetooth Coexistence Mode: Active-high signal used to indicate to the module that an external Bluetooth IC is transmitting. Not supported in the current firmware.
49.	GPIO_21/PS_SLP_0	81	31	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Output	Power Save Mode: This signal is used to indicate to the Host processor when the module enters (logic low) and exits (logic high) the LP and ULP Sleep modes when the GPIO Handshake mode is enabled. For ULP mode, connect a 100 kΩ pull-down

S.No	Pin Name	Pin # in RS9113-N00-D0F	Pin # in RS9113-N00-D1F	Direction	Description
					resistor. For ULP mode, the ULP_GPIO_1 signal, if available in the package, may be used instead of GPIO_21 for the same purpose but without the need for the pull-down resistor.
50.	ULP_GPIO_0/ULP_WAKEUP	3	2	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Input	Power Save Mode: Active-high input to indicate that the module should exit its Ultra low power sleep mode – connect a 100 kΩ pull-down resistor if the host is not controlling this signal at all times.
51.	ULP_GPIO_1/PS_SLP_1	68	---	Inout	GPIO Mode: Reserved – leave this pin unconnected.
				Output	Power Save Mode: This signal is used to indicate to the Host processor when the module enters (logic low) and exits (logic high) the ULP Sleep mode. The GPIO_21 signal may be used for the same purpose in case the package does not have the ULP_GPIO_1 signal available – GPIO_21 will need a pull-down resistor.
52.	ULP_GPIO_2	99	---	Inout	Reserved – leave this pin unconnected.
53.	ULP_ANAGPI	73	50	Input	Reserved – leave this pin unconnected.
Host Selection Interface[10]					
54.	HOST_SEL_0	60	36	Inout	SDIO Mode: Leave unconnected. SPI Mode: Connect a 4.7 kΩ pull-down resistor. USB Mode: Leave unconnected.

[10]These are bootstrap signals and should not be actively driven to logic high or logic low by an external source. They should either be left unconnected or pulled down with a 4.7 kΩ resistor as per their descriptions.

S.No	Pin Name	Pin # in RS9113-N00-D0F	Pin # in RS9113-N00-D1F	Direction	Description
					USB-CDC Mode: Leave unconnected. UART Mode: Connect a 4.7 kΩ pull-down resistor.
55.	HOST_SEL_1	55	35	Inout	SDIO Mode: Leave unconnected. SPI Mode: Leave unconnected. USB Mode: Connect a 4.7 kΩ pull-down resistor. USB-CDC Mode: Connect a 4.7 kΩ pull-down resistor. UART Mode: Connect a 4.7 kΩ pull-down resistor.
56.	BOOTMODE_0	40	20	Inout	SDIO Mode: Leave unconnected. SPI Mode: Leave unconnected. USB Mode: Connect a 4.7 kΩ pull-down resistor. USB-CDC Mode: Leave unconnected. UART Mode: Leave unconnected.
Miscellaneous Signals					
57.	HOST_BB_EN	94	39	Output	Control signal used to indicate the entry (logic low) and exit (logic high) of the module into ULP mode. May be used to control an external Load Switch and/or DC-DC for switching off the 3.3V supplies (other than VBATT) and reduce current consumption in ULP Mode. Refer to the Module Integration Guide for more details.
58.	JP0	69	47	Input	Reserved – connect a 4.7 kΩ pull-down resistor.
59.	JP1	70	48	Input	Reserved – connect a 4.7 kΩ pull-down resistor.
60.	JP2	96	45	Input	Reserved – connect a 4.7 kΩ pull-down resistor.
61.	JNC	97	46	Output	Reserved – leave this pin unconnected.

S.No	Pin Name	Pin # in RS9113-N00-D0F	Pin # in RS9113-N00-D1F	Direction	Description
62.	AUX_DAC_OUT	93	38	Output	Reserved – leave unconnected.
63.	AUX_ADC_IN0	65	44	Input	Reserved – leave unconnected.
64.	BOOTLOAD_EN	41	27	Inout	Reserved – leave unconnected.
65.	XTAL_32KHZ_N	5	4	Input	Reserved – leave unconnected.
66.	XTAL_32Khz_P	4	3	Input	Reserved – leave unconnected.
67.	EXT_PA_ON	64	---	Output	Reserved – leave unconnected.
68.	WURX	2	1	Input	Reserved – leave unconnected.
69.	PDN	58	---	Input	Reserved – connect to 100kΩ pull-down resistor.
70.	NC	31, 39,46, 54, 56, 61, 62, 72, 89, 95	---	NC (No Connect)	Leave unconnected.

Table 4: Pin Descriptions

In the case of the RS9113-N00-D0F and RS9113-N00-D1F modules (FIPS 140-2 certified modules), the JP0, JP1, JP2 pins need to tied low permanently and the JNC pin should be NC. This requirement is part of the "Cryptographic Officer Guidance" document that forms part of the collateral for the FIPS 140-2 certified modules.

5 Specifications

5.1 Absolute Maximum Ratings

Absolute maximum ratings in the table given below are the values beyond which the device could be damaged. Functional operation at these conditions or beyond these conditions is not guaranteed.

Parameter	Symbol	Value	Units
Input digital supply voltages	VIN_MOD, SDIO_VDD_18_33	3.6	V
USB VBUS voltage	USB_VBUS	5	V
Input analog supply voltage	ANA33	3.6	V
Input analog voltage for USB	USB_VDDA	3.6	V
Input digital voltage for USB	USB_VDDS	3.6	V
Input analog supply voltage for RF	VRF33	3.6	V
Input digital supply voltage for RF	VDD33	3.6	V
Input digital supply voltage for ultra-low power deep sleep related sections	VBATT	3.6	V
RF Input Level	RF_OUT_1, RF_OUT_2	10	dBm
Storage temperature	T_{store}	-65 to 150	°C
Operating temperature range	T_{op}	-40 to 85	°C
Electrostatic discharge tolerance (HBM)	ESD_{HBM}	2000[11]	V
Electrostatic discharge tolerance (CDM)	ESD_{CDM}	500	V
Electrostatic discharge tolerance (MM)	ESD_{MM}	60	V
Maximum Current consumption in TX mode	I_{max}	500	mA

Table 5: Absolute Maximum Ratings

[11] ESD Tolerance for HBM is 2000V for all pins except WURX. For WURX the tolerance is 1500V

5.2 Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Input digital supply voltages	VIN_MOD, SDIO_VDD_18_33	3.0	3.3	3.6	V
Input analog supply voltage	ANA33	1.9	3.3	3.6	V
Input analog voltage for USB	USB_VDDA	3.0	3.3	3.6	V
Input digital voltage for USB	USB_VDDS	3.0	3.3	3.6	V
Input analog supply voltage for RF	VRF33	3.0	3.3	3.6	V
Input digital supply voltage for RF	VDD33	3.0	3.3	3.6	V
Input digital supply voltage for ultra-low power deep sleep related sections	VBATT	1.8	3.3	3.6	V
Ambient Temperature	T_a	-40	25	85	°C

Table 6: Recommended Operating Conditions

5.3 Reliability Qualification

The modules have been stress-tested for High Temperature Operating Life as per the JEDEC standard JESD22-A108D. The following are the details of the tests.

Parameters	Values/Details
Ambient Temperature	110°C
Junction Temperature	125°C
Supply Voltage	3.6V
Operational mode	Regular Ping with no power save modes activated.
Stress Duration	1000 hours
Number of Modules Tested	3 lots of 80 modules each
Intervals at which modules were removed from Temperature chamber for testing	168, 360, 720 and 1000 hours
Duration of the Tests (duration for which modules were kept outside the chamber)	12 to 13 hours

Parameters	Values/Details
Testing performed at each interval	1) Receive Sensitivity in Channels 1 and 11 for 1 Mbps, 6 Mbps and 54 Mbps data rates 2) Transmit power level and EVM in Channels 1 and 11 for 1 Mbps, 6 Mbps and 54 Mbps data rates 3) Peak current consumption in Transmit and Receive modes
Number of failed modules	Zero

Table 7: HTOL Based Stress Testing

The stress testing as per the JEDEC JESD22-A108D standard enables us to predict the operating life of the modules from the acceleration factor calculated using the Arrhenius equation as per JEDEC JEP122G. The Arrhenius equation is as follows:

$$A_T = \lambda_{T1} / \lambda_{T2} = exp[(-E_{aa}/k)(1/T_1 - 1/T_2)]$$

where[12]

A_T = Acceleration Factor

E_{aa} = Appaprent activation energy (eV). 0.75eV is a conservative industry standard

k = Boltzmann's constant (8.62×10^{-5} eV/K)

T_1 = Temperature at use, in Kelvin

T_2 = Temperature at stress, in Kelvin

Using the data from the HTOL Based Stress Testing and assuming a junction temperature of 55°C for a use case scenario, we can safely assume an operating life of >9 years. The junction temperature for the module's ICs is usually 15 to 20°C more than the ambient temperature.

5.4 DC Characteristics – Digital I/O Signals

Parameter	Min.	Typ.	Max.	Units
Input high voltage	2	-	3.6	V
Input low voltage	-0.3	-	0.8	V
Output low voltage	-	-	0.4	V
Output high voltage	2.4	-	-	V
Input leakage current (at 3.3V or 0V)	-	-	±10	µA
Tristate output leakage current (at 3.3V or 0V	-	-	±10	µA

Table 8: Input/Output DC Characteristics

[12] Refer to the JEDEC JEP122G standard for more details on each parameter of the equation

5.5 AC Characteristics

5.5.1 SPI Slave (Host SPI) Interface

5.5.1.1 Low Speed Mode

Parameter	Symbol	Min.	Typ.	Max.	Units
SPI Clock Period	T_{spi}	40	-	-	ns
SPI_CSN to Output Valid time	T_{cs}	-	-	7.5	ns
SPI_CSN Setup Time	T_{cst}	5	-	-	ns
SPI_MOSI Setup Time	T_{sd}	1.5	-	-	ns
SPI_MOSI Hold Time	T_{hd}	1	-	-	ns
SPI_MISO Clock-to-Output-Valid time	T_{od}	-	-	10	ns
Output Load		0	-	10	pF

Table 9: AC Characteristics – Slave SPI Low Speed Mode

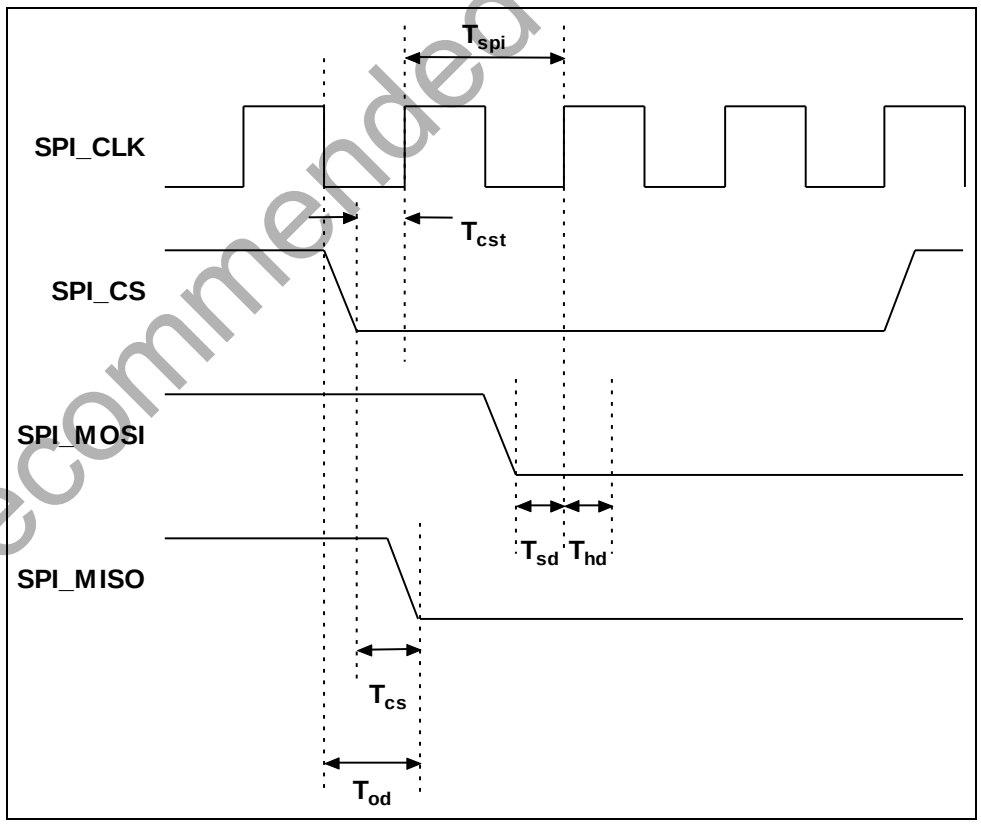


Figure 10: Slave SPI Interface Timings – Low Speed Mode

5.5.1.2 High Speed Mode

Parameter	Symbol	Min.	Typ.	Max.	Units
SPI Clock Period	T_{spi}	12.5	-	-	ns
SPI_CSN to Output Valid time	T_{cs}	-	-	7.5	ns
SPI_CSN Setup Time	T_{cst}	5	-	-	ns
SPI_MOSI Setup Time	T_{sd}	1	-	-	ns
SPI_MOSI Hold Time	T_{hd}	1	-	-	ns
SPI_MISO Clock-to-Output-Valid time	T_{od}	2.5	-	8.75	ns
Output Load		0	-	10	pF

Table 10: AC Characteristics – Slave SPI High Speed Mode

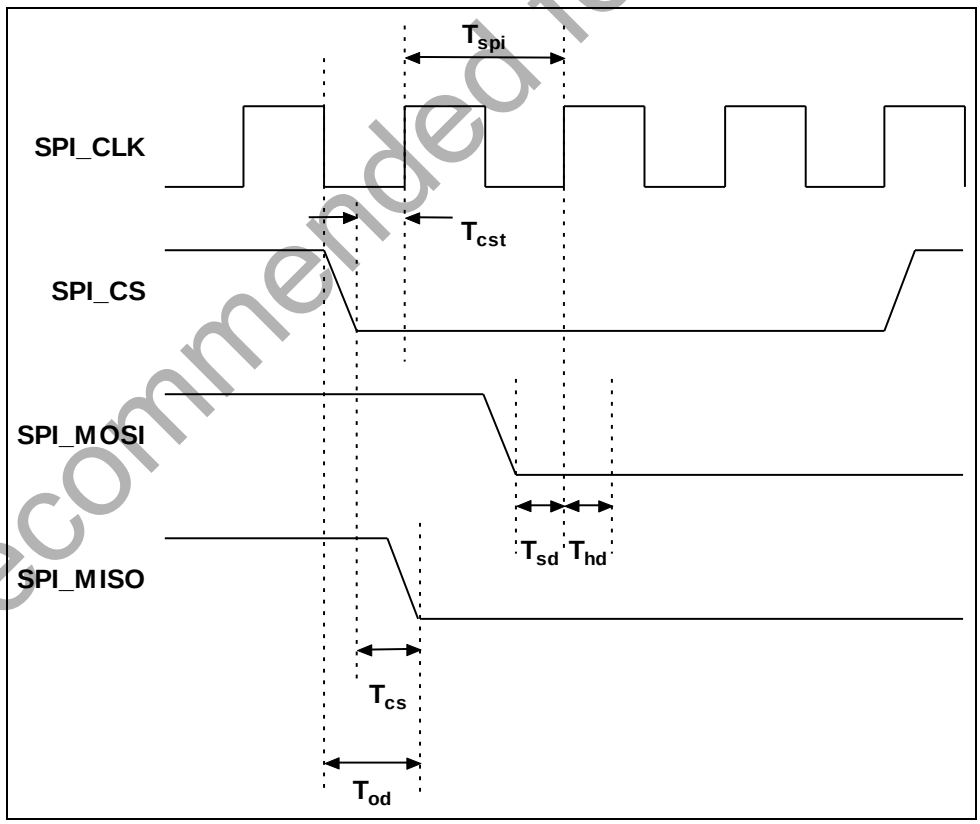


Figure 11: Slave SPI Interface Timings – High Speed Mode

5.5.2 USB Interface

5.5.2.1 Timing Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
trise	1.5 Mbps 12 Mbps 480 Mbps	75 4 0.5	- - -	300 20 -	ns
tfall	1.5 Mbps 12 Mbps 480 Mbps	75 4 0.5	- - -	300 20 -	ns
Jitter	1.5 Mbps 12 Mbps 480 Mbps	- - -	- - -	10 1 0.2	ns

Table 11: Timing Characteristics for USB Interface

5.5.2.2 Electrical Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Vcm DC (DC level measured at receiver connector)	HS Mode LS/FS Mode	-0.05 0.8	- -	0.5 2.5	V
Crossover Voltages	LS Mode FS Mode	1.3 1.3	- -	2 2	V
Power supply ripple noise (Analog 3.3V)	< 160 MHz	-50	-	50	mV

Table 12: Electrical Characteristics for USB Interface

5.5.2.3 Voltage Thresholds

Parameter	Min.	Typ.	Max.	Units
A-Device Session Valid	0.8	1.4	2.0	V
B-Device Session Valid	0.8	1.4	4.0	V
B-Device Session End	0.2	0.45	0.8	V

Table 13: Input/Output DC Characteristics

5.5.3 Reset Timing

The figure below shows the requirement for the Reset assertion time during power up and during module operation.

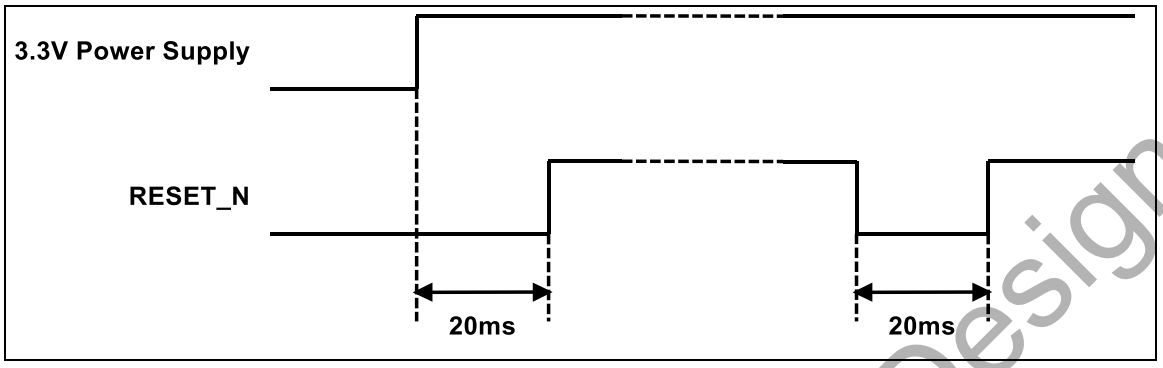


Figure 12: Reset Timing

5.6 Performance Specifications

5.6.1 WLAN Performance Specifications

All measurements are at antenna (cable loss is compensated).

5.6.1.1 WLAN 2.4 GHz Receiver Characteristics

Parameter	Condition	Min.	Typ.	Max.	Units
Sensitivity for 20MHz Bandwidth[13]	1 Mbps DSSS		-95.5		dBm
	2 Mbps DSSS		-90.5		dBm
	5.5 Mbps CCK		-88.0		dBm
	11 Mbps CCK		-86.5		dBm
	6 Mbps OFDM		-91.5		dBm
	9 Mbps OFDM		-90.0		dBm
	12 Mbps OFDM		-89.0		dBm
	18 Mbps OFDM		-87.0		dBm
	24 Mbps OFDM		-84.0		dBm
	36 Mbps OFDM		-80.5		dBm
	48 Mbps OFDM		-76.5		dBm
	54 Mbps OFDM		-74.5		dBm
	MCS0 Mixed Mode		-90.0		dBm
	MCS1 Mixed Mode		-88.0		dBm
	MCS2 Mixed Mode		-85.5		dBm

[13] All Sensitivity numbers are at < 10% PER limit. Packet sizes are 1024 bytes for 802.11 b/g data rates and 4096 bytes for 802.11n data rates.

Parameter	Condition	Min.	Typ.	Max.	Units
	MCS3 Mixed Mode		-83.0		dBm
	MCS4 Mixed Mode		-79.5		dBm
	MCS5 Mixed Mode		-75.0		dBm
	MCS6 Mixed Mode		-73.0		dBm
	MCS7 Mixed Mode		-71.5		dBm
Maximum Input Level for PER below 10%	1 Mbps DSSS		-4		dBm
	11 Mbps CCK		-4		dBm
	54 Mbps OFDM		-16		dBm
	MCS0 Mixed Mode		-15		dBm
Adjacent Channel Rejection[14]	1 Mbps DSSS		35		dB
	11 Mbps CCK		32		dB
	6 Mbps OFDM	32			dB
	54 Mbps OFDM	18			dB
PER Floor				0.1	%
RSSI Accuracy			±1	±3	dB

Table 14: WLAN 2.4 GHz Receiver Characteristics

5.6.1.2 WLAN 2.4 GHz Transmitter Characteristics[15]

Parameter	Condition	Min.	Typ.	Max.	Units
Transmit Power for 20MHz Bandwidth, compliant with IEEE mask and EVM	1 Mbps DSSS		17		dBm
	2 Mbps DSSS		17		dBm
	5.5 Mbps CCK		17		dBm
	11 Mbps CCK		17		dBm
	6 Mbps OFDM		17		dBm
	9 Mbps OFDM		17		dBm

[14] Sensitivity level +3 dBm is used.
[15] The transmit powers are valid when the module is operating in the Worldwide mode. The transmit power across channels is modified to comply with the region wise regulatory specifications. Module-to-module variation is upto 2 dBm.

Parameter	Condition	Min.	Typ.	Max.	Units
	12 Mbps OFDM		17		dBm
	18 Mbps OFDM		17		dBm
	24 Mbps OFDM		17		dBm
	36 Mbps OFDM		17		dBm
	48 Mbps OFDM		16		dBm
	54 Mbps OFDM		15		dBm
	MCS0 Mixed Mode		16		dBm
	MCS1 Mixed Mode		16		dBm
	MCS2 Mixed Mode		16		dBm
	MCS3 Mixed Mode		16		dBm
	MCS4 Mixed Mode		16		dBm
	MCS5 Mixed Mode		16		dBm
	MCS6 Mixed Mode		15		dBm
	MCS7 Mixed Mode		13		dBm

Table 15: WLAN 2.4 GHz Transmitter Characteristics

5.6.1.3 WLAN 5 GHz Receiver Characteristics

Parameter	Condition	Min.	Typ.	Max.	Units
Sensitivity for 20MHz Bandwidth	6 Mbps OFDM		-90.0		dBm
	9 Mbps OFDM		-89.0		dBm
	12 Mbps OFDM		-88.5		dBm
	18 Mbps OFDM		-86.5		dBm
	24 Mbps OFDM		-83.5		dBm
	36 Mbps OFDM		-80.0		dBm
	48 Mbps OFDM		-76.0		dBm
	54 Mbps OFDM		-74.0		dBm
	MCS0 Mixed Mode		-89.5		dBm
	MCS1 Mixed Mode		-88.0		dBm

Parameter	Condition	Min.	Typ.	Max.	Units
	MCS2 Mixed Mode		-85.5		dBm
	MCS3 Mixed Mode		-82.5		dBm
	MCS4 Mixed Mode		-79.0		dBm
	MCS5 Mixed Mode		-74.5		dBm
	MCS6 Mixed Mode		-73.0		dBm
	MCS7 Mixed Mode		-71.0		dBm
Maximum Input Level	54 Mbps OFDM		-15		dBm
	MCS0 Mixed Mode		-15		dBm
Adjacent Channel Rejection	6 Mbps OFDM		32		dB
	54 Mbps OFDM		18		dB
PER Floor			0.1		%
RSSI Accuracy			±1	±3	dB

Table 16: WLAN 5 GHz Receiver Characteristics

5.6.1.4 WLAN 5 GHz Transmitter Characteristics[16]

Parameter	Condition	Min.	Typ.	Max.	Units
Transmit Power for 20MHz Bandwidth, compliant with IEEE mask and EVM	6 Mbps OFDM		10		dBm
	9 Mbps OFDM		10		dBm
	12 Mbps OFDM		10		dBm
	18 Mbps OFDM		10		dBm
	24 Mbps OFDM		10		dBm
	36 Mbps OFDM		10		dBm
	48 Mbps OFDM		9		dBm
	54 Mbps OFDM		8		dBm
	MCS0 Mixed Mode		9		dBm
	MCS1 Mixed Mode		9		dBm
	MCS2 Mixed Mode		9		dBm

[16] The actual transmit power levels might differ in different regions and channels based on the regulatory constraints.

Parameter	Condition	Min.	Typ.	Max.	Units
	MCS3 Mixed Mode		9		dBm
	MCS4 Mixed Mode		9		dBm
	MCS5 Mixed Mode		9		dBm
	MCS6 Mixed Mode		8		dBm
	MCS7 Mixed Mode		7		dBm

Table 17: WLAN 5 GHz Transmitter Characteristics

5.7 Regulatory Specifications

The modules has been certified for FCC, IC and CE/ETSI. Note that any changes to the module's configuration including (but not limited to) the programming values of the RF Transceiver and Baseband can cause the performance to change beyond the scope of the certification. These changes, if made, may result in the module having to be certified afresh.

The table below lists the details of the regulatory certifications. The certification for geographies not listed in the table is in progress.

Regulatory Certification	Grantee Code	Product Code	Description
FCC	XF6	RS9113DB	Dual-band Module
IC	8407A	RS9113DB	Dual-band Module

Table 18: Regulatory Certifications

NOTE: The part number and other details are available in the Module Marking and Ordering Information section.

5.8 Antenna Specifications

The RS9113 FIPS 140-2 Dual band with antenna module have been certified for FCC, IC, ETSI/CE and TELEC with Silicon Labs' Dual-band PCB antenna. The sections that follow list down the performance specifications of the PCB antenna.

5.8.1 Return Loss Characteristic of the Antenna

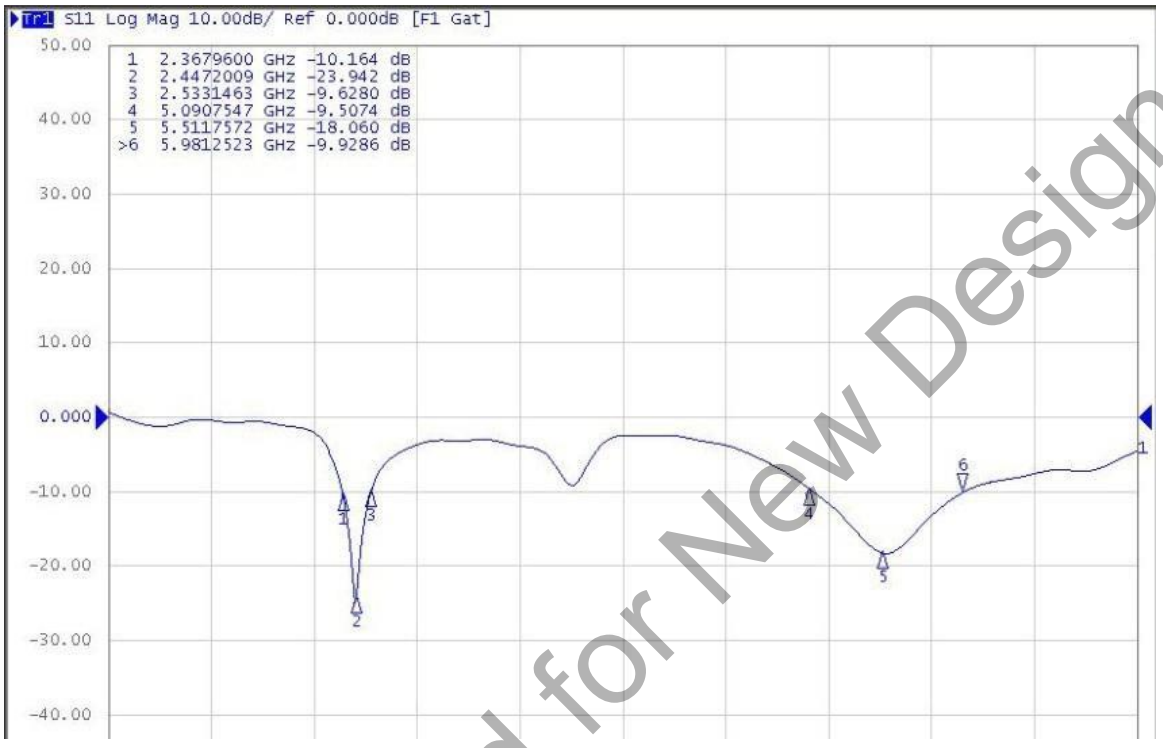


Figure 13:Return Loss Characteristic of the Antenna

5.8.2 Module Reference Orientation

Figure 14: Module Reference Orientation

5.8.3 Gain Plots

5.8.3.1 XY at 2.43 GHz

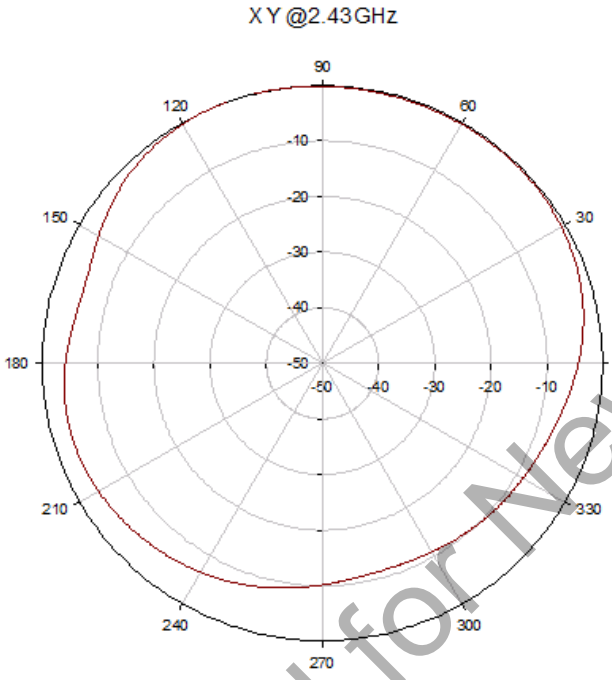


Figure 15: 2D Gain Plot for XY at 2.43 GHz

5.8.3.2 YZ at 2.43 GHz

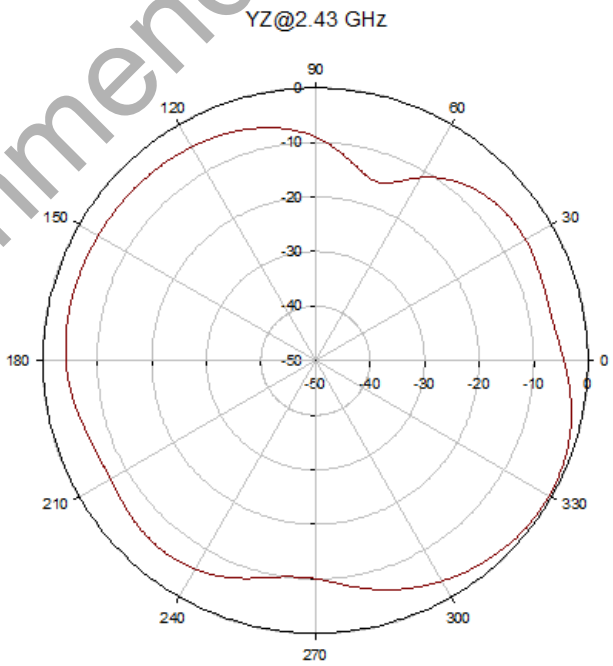


Figure 16: 2D Gain Plot for YZ at 2.43 GHz

5.8.3.3 ZX at 2.43 GHz

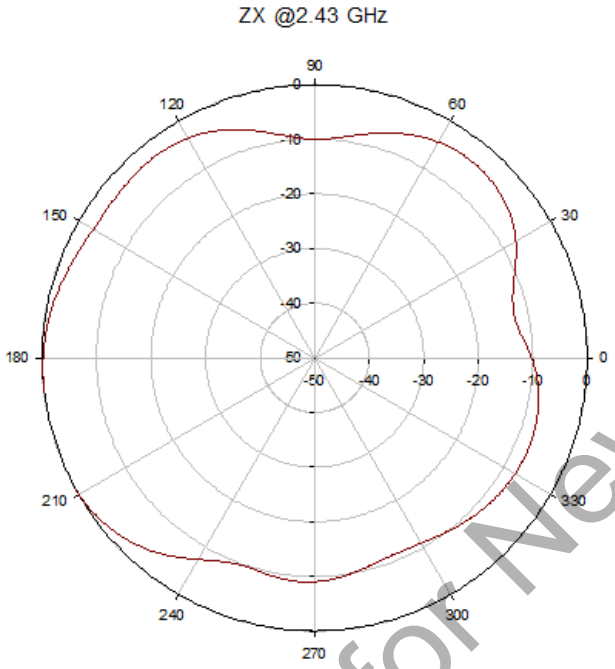


Figure 17: 2D Gain Plot for ZX at 2.43 GHz

5.8.3.4 XY at 5.5 GHz

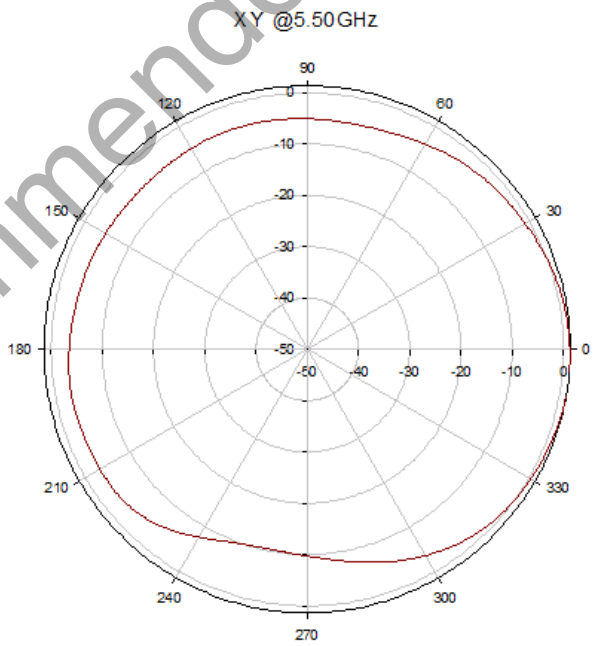


Figure 18: 2D Gain Plot for XY at 5.5 GHz

5.8.3.5 YZ at 5.5 GHz

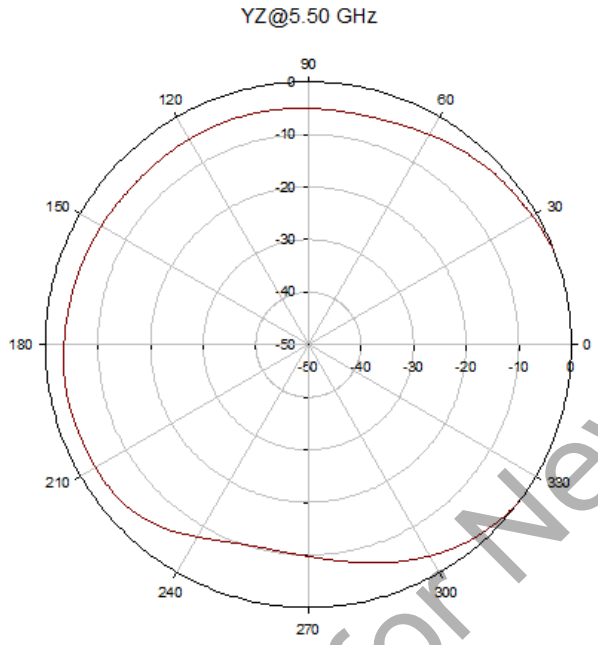


Figure 19: 2D Gain Plot for YZ at 5.5 GHz

5.8.3.6 ZX at 5.5 GHz

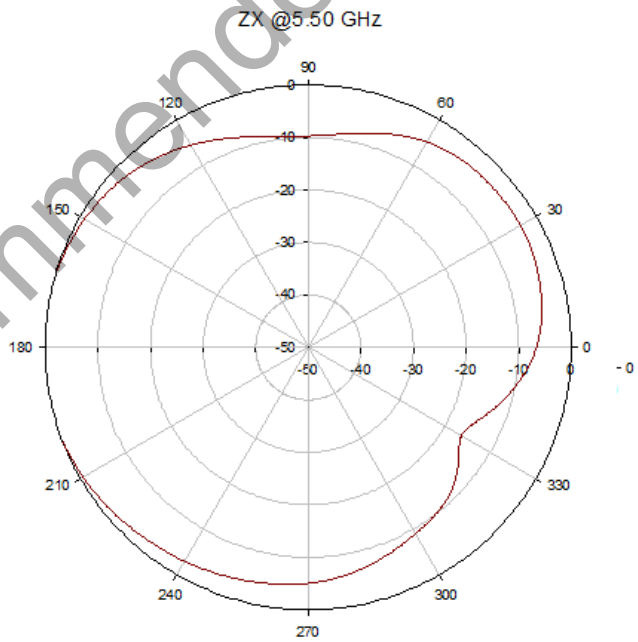


Figure 20: 2D Gain Plot for ZX at 5.5 GHz

5.8.4 Antenna Parameters

Parameter	@ 2.43 GHz	@ 5.5 GHz
Peak Gain	0.99 dBi	4.42 dBi
Average Efficiency	87 %	85 %

Table 19: Antenna Parameters

6 Software Architecture

The figure below illustrates the software architecture of the RS9113 FIPS 140-2 module.

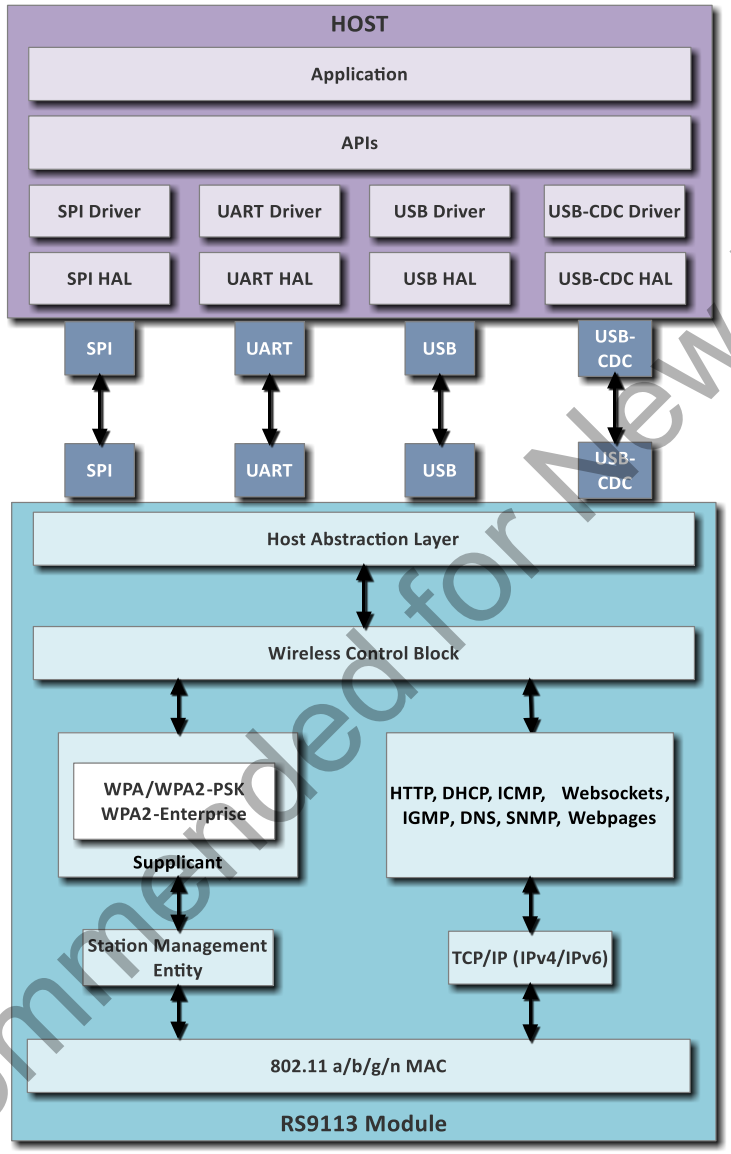


Figure 21: Software Architecture for the RS9113 FIPS 140-2 Level 1 Certified Module

As shown in the figure above, the module is integrated with the host using the SPI, UART, USB or USB-CDC interface. The module receives all configuration commands from the Host and transfers data to or receives data from the host through this interface.

The module incorporates WPA/WPA2-PSK, WPA/WPA2-Enterprise (EAP-TLS, EAP-TTLS, EAP-PEAP) Security and Wi-Fi Client Mode stack along with a feature-rich TCP/IP stack. The module offers the option to bypass its internal TCP/IP stack and use the TCP/IP stack in the Host processor.

7 Module Marking and Ordering Information

7.1 Module Marking Information

The figure below illustrates the marking on the modules.

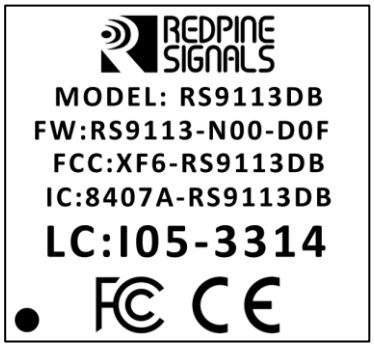


Figure 22: Module Marking Information

The table below explains the marking on the modules.

Marking	Description
RS9113DB	Model Number for Dual-band module
RS9113-N00-D0F RS9113-N00-D1F	Software/Firmware supported.
XF6-RS9113DB	FCC Grant IDs for Dual-band module.
8407A-RS9113DB	IC Grant IDs for Dual-band module.
ABC-WWYY	Lot Code Information: ABC – Internal usage WW – Week of manufacture YY – Year of manufacture
FC	FCC Compliance Mark
CE	CE Compliance Mark

Table 20: Module Marking Information

7.2 Ordering Information

The RS9113 FIPS 140-2 module is presently offered with two part numbers:

- RS9113-N00-D0F
- RS9113-N00-D1F[17]

[17] Contact Redpine for certification status.

7.3 Collateral

The following documentation and software are available along with the RS9113 FIPS 140-2 modules.

- Module Integration Guide
- API's for supported interfaces.
- API User Guide
- Software Programming Reference manual (PRM).
- Evaluation Kit (EVK)
- EVK User Guide
- FIPS Security Policy and Cryptographic Officer Guidance Manual

7.4 Packing Information

The modules are packaged and shipped in Trays.

Each tray for the FIPS 140-2 without antenna Module package can accommodate 84 modules. The mechanical details of the tray for the FIPS 140-2 without antenna Module package are given in the figure below.

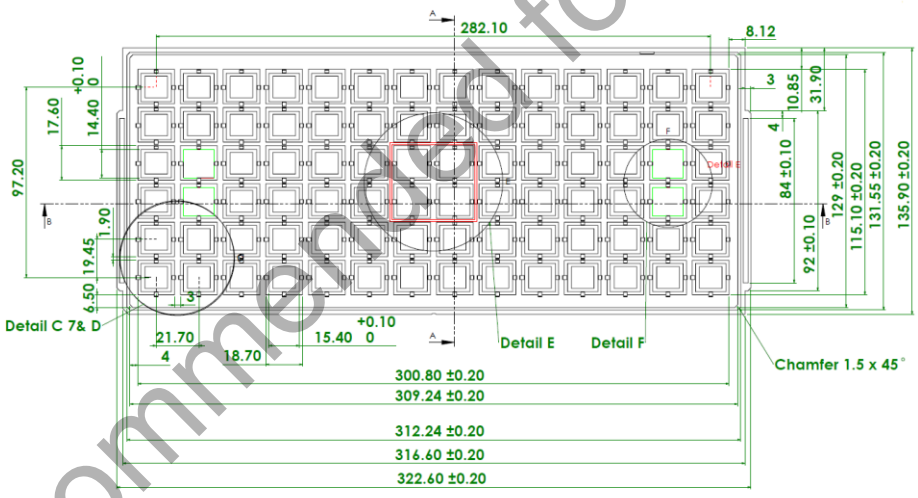


Figure 23: Mechanical Details of Tray for FIPS 140-2 without antenna Module package

Each tray for the FIPS 140-2 with antenna Module package can accommodate 70 modules. The mechanical details of the tray for the FIPS 140-2 with antenna Module package are given in the figure below.

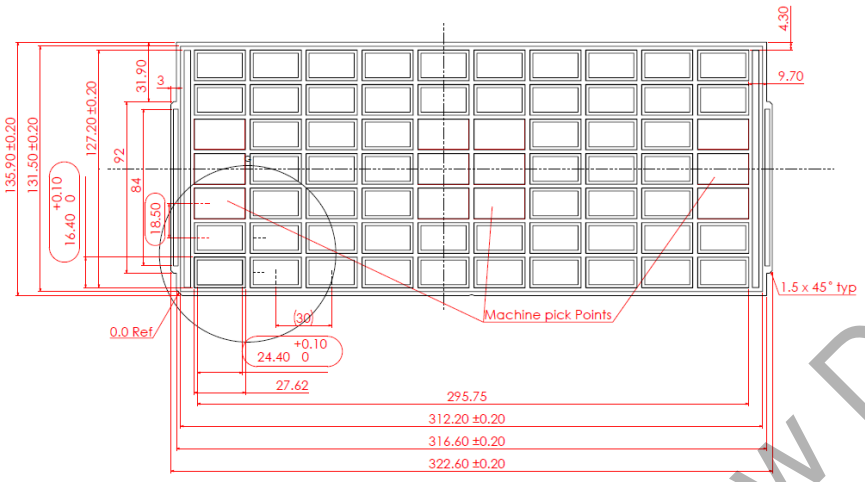
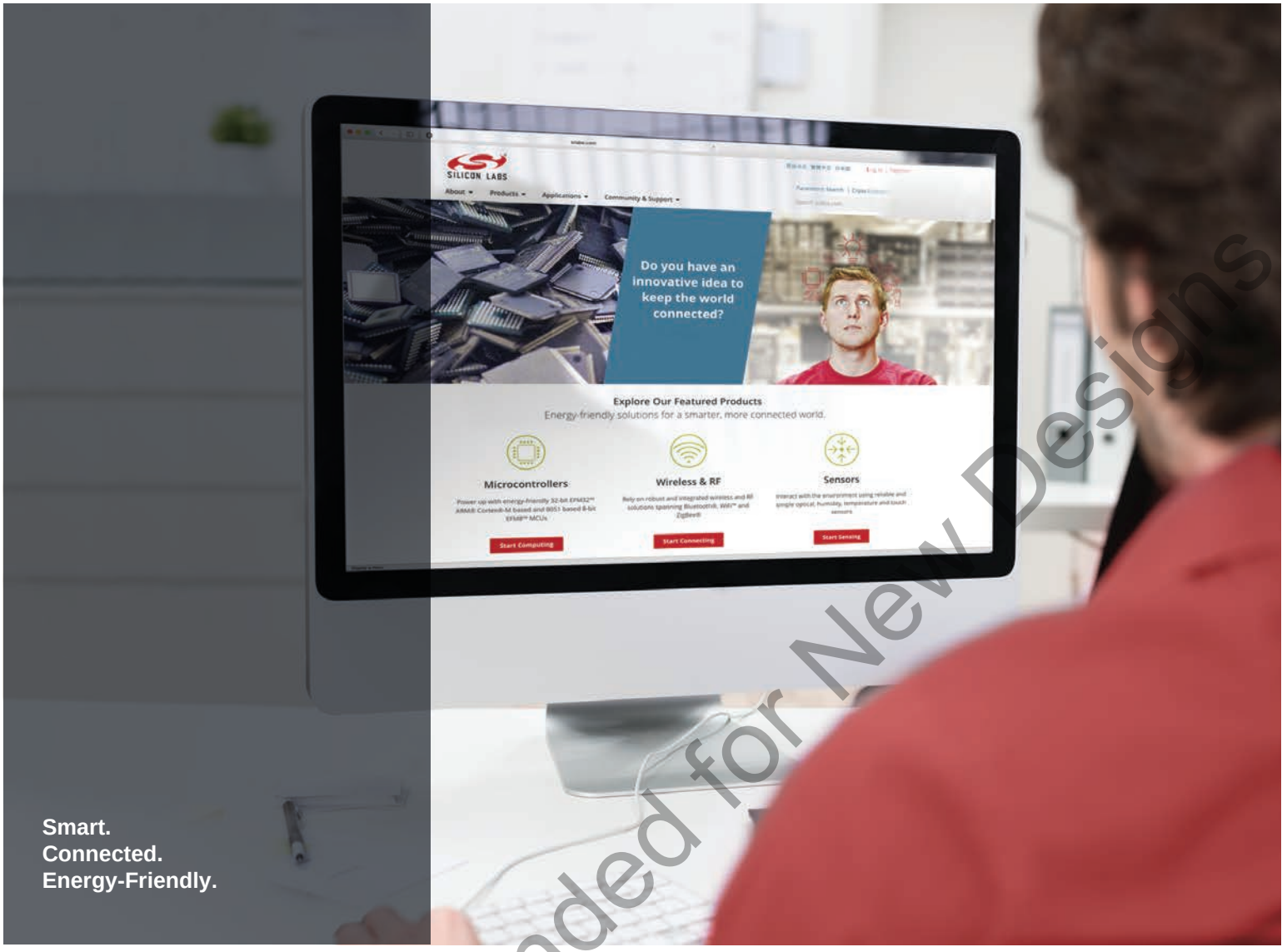


Figure 24: Mechanical Details of Tray for FIPS 140-2 with antenna Module Package

Revision History

Revision No.	Version No.	Date	Changes
1.	1.0	July 2015	Initial version.
2.	1.1	November 2017	1. Added the details of the FIPS 140-2 certified module with integrated antenna. 2. Updated Tolerance Level for Mechanical Dimensions from ±0.1mm to ±0.2mm. 3. Corrected pin numbers of JP1, JP2 and JNC signals for module without antenna in the Pin Description table.



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