Si4455 Low-Power PA Matching

1. Introduction

This application note provides a description of the matching techniques applied to the low-power Si4455 RFIC family. The typical power regime of the Si4455 is primarily devoted to +10 dBm applications, but it is also able to achieve 12 to 13 dB if required.

The matching network has a number of goals:

- Target a nominal output power level of +10 to +13 dBm
- Minimize current consumption (i.e., maximize efficiency)
- Constrain the peak voltage at the drain of the output devices
- Compliance with ETSI and FCC specifications for spurious emissions
- Best possible immunity to the effects of termination impedance variations
- Low variation over temperature and supply voltage
- Low BOM and cost

Silicon Labs provides switched PA mode Class E (CLE) type matching network for the Si4455 RFICs which are documented in this Application Note.

The CLE type has the best efficiency but higher V_{DD} and temperature variations. Its current consumption and the peak voltage on the TX pin are sensitive to termination impedance variations.

To some extent, the high V_{DD} variation can be cured efficiently at low power levels (e.g., 10 dBm) by the so-called adaptive power setting method. In this method, the match is designed in such a way that the specified power at the specified supply voltage is achieved at a relatively low power level setting. At decreasing supply voltage (e.g. due to a discharging battery) the power drop can be compensated by the proper increase of the power level setting i.e. with the decrease of the switcher loss. Unfortunately, it works well only at lower power regimes where a low power level setting is enough to get the targeted power and thus, there is room for compensation.

A low power setting (at low power regimes) with higher switcher loss is also useful for immunity against termination antenna impedance variations. It especially reduces the variation of the DC current consumption with variable environmental conditions suffered by the antenna, which is advantageous in long-life, battery-operated applications, such as meters or sensors, since the excess current drain is limited.

The CLE matching procedure outlined in this document allows for achieving the above-mentioned properties and is applicable to two different types of board configurations: one with separate antennas for the TX and RX paths (Split TX/RX board configuration) and one with a single antenna and the TX and RX paths tied directly together without the use of an RF switch (Direct Tie board configuration). The differences in the matching procedure required for the two board configurations are discussed in detail.

The next section is provided for users more interested in quickly obtaining matching component values than the methodology used to develop the matching network. The methodology is described in detail in Sections 3 and 4.

2. Summary of Matching Network Component Values

Some users are not greatly interested in the theoretical development of matching networks; rather, they are concerned with quickly obtaining a set of component values for a desired frequency of operation. For those users, component values for CLE matching network for multiple frequencies and power levels across the operating range of the Si4455 RFIC are summarized here.

The matching networks may be realized with either wire-wound SMD inductors or multi-layer SMD inductors. The cost of a multi-layer inductor is significantly lower than that of a wire-wound inductor, and, thus, in cost-sensitive applications, the multi-layer solution is preferred. However, the performance of a circuit realization using only wire-wound inductors is generally better due to higher Qs and lower ohmic losses than multi-layer inductors of equivalent value. Due to the increased loss, a design using multilayer inductors typically requires a higher power level setting and thus exhibits a slight increase in current consumption for the same amount of output power.

Also multilayer SMD inductors are often available only in coarser-spaced inductance values, which may cause a higher deviation than the ideal class E values, especially in Direct Tie solutions where significant adjustments of the value of L0 are usually necessary in order to avoid degradation of RX sensitivity; this may be more difficult with only the set of values available for a multi-layer series of inductors.

The component values shown in the following tables are appropriate for a supply voltage of V_{DD} = 3.3 V.

For other V_{DD} voltages, the 10 dBm Si4455 needs adjustment of the PA power level (adaptive power control), which, to some extent, can compensate the power variations. However, for 12 to 13 dBm Si4455 designs, the power setting is close to maximum, and, thus, the margin for power variation compensation is very limited.

The Si4455 PA has 79 MOS switching fingers, so the DDAC register can go up to 4Fh. Its typical output capacitance is 1.25 pF independent of the DDAC setting due to its cascade architecture.

The component values shown in the subsections below are appropriate when using 0402-size SMD components, such as the 0402HP-series of wire-wound inductors from CoilCraft and the LQG15HS-series multilayer inductors and GRM15-series ceramic capacitors from Murata. These values are appropriate for use on the official Split TX/RX and Direct Tie reference board designs available on the Silicon Labs web site. It is likely that the presented solutions operate satisfactorily with 0603-size SMD elements as well.

Surface-mount 0603-size or 0402-size components themselves contain parasitic elements that modify their effective values at the frequency of interest. Furthermore, it is convenient to use the nearest-available 5% or 10% component values rather than the exact component values predicted by Filter Design CAD software or filter prototype tables. Additionally, any printed circuit board layout has parasitics, such as trace inductance, component pad capacitance, etc. This means that it will almost certainly be necessary to fine-tune the final matching values for the user's specific application and board layout. The above component values should be used as starting points, and the values should be modified slightly to zero-in on the best filter response and impedance match to 50 Ω.

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2.1. Component Values for Si4455 Matching

The Si4455 CLE matching is best for the 10 dBm power range. Here, the CLE has enough margin to be stable over V_{DD} with adaptive power control. The efficiency is very good, and the total current is typically 17 mA.

The 13 dBm regime can also be achieved with this type of matching, but has high variation over supply voltage since adaptive power control is no longer efficient due to the power setting here, which is close to the maximum.

2.1.1. Si4455 CLE Split TX/RX Board Configuration: Component Values and Performance

Table 1 provides the component values required for output power levels for +10 and +13 dBm using the Split CLE TX/RX board configuration of Figure 1 and a supply voltage of V_{DD} = 3.3 V. The matching's listed in Table 1 are for wire-wound inductors. For other frequencies, consult with a Silicon Labs representative. Split TX Matches using multilayer type inductors are not yet developed. For those, use the TX part of the DT matches with multilayer inductors (see Table 3).

Table 1. TX Match Network Component Values vs. Frequency
(Split Si4455 CLE TX/RX Board, VDD= 3.3 V, Wire-Wound Inductor Versions)

Pout = +10 dBm										
Freq Band	L_{choke}	C0	L0	CM	LM	CM2	LM2	CM3	LM3	RDC
434 MHz	220 nH	18 pF	56 nH	8.2 pF	18 nH	15.0 pF	18 nH	8.2 pF	0 Ω	0 Ω
868 MHz	120 nH	33 pF	8.2 nH	5.1 pF	6.8 nH	10 pF	6.8 nH	5.1 pF	0 Ω	0 Ω
Pout = +13…14 dBm										
Freq Band	L_{choke}	C0	L0	CM	LM	CM2	LM2	CM3	LM3	RDC
434 MHz	220 nH	10 pF	56 nH	10 pF	18 nH	15 pF	18 nH	8.2 pF	0 Ω	0 Ω
868 MHz	120 nH	3.6 pF	19 nH	2.7 pF	9.1 nH	5.1 pF	9.1 nH	2.7 pF	0 Ω	0 Ω
863-921 MHz	120 nH	3.0 pF	18 nH	5.1 pF	6.8 nH	10 pF	6.8 nH	5.1 pF	0 Ω	0 Ω
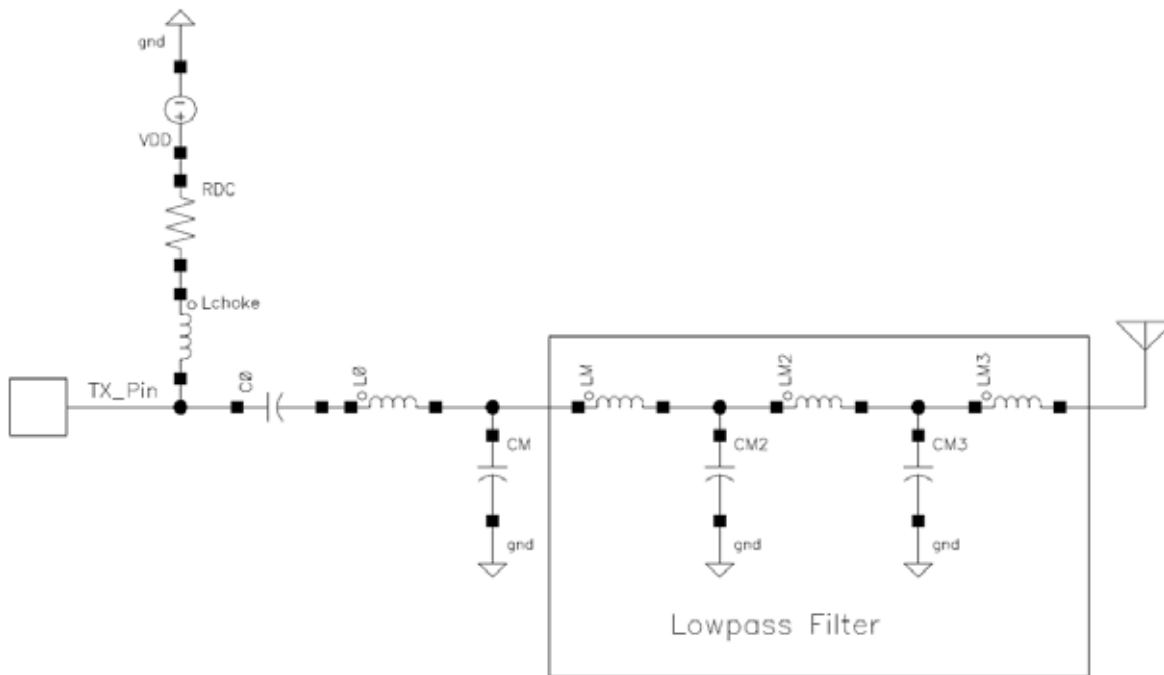
Figure 1. TX Matching Topology for Si4455 Split TX/RX Board CLE Configuration

A summary of typical measured output power and current consumption for split board configurations with wire-wound inductors is given in Table 2. These results were obtained with a supply voltage of V_{DD} = 3.3 V.

Table 2. Output Power and Current Consumption vs. Frequency
(Split Si4455 CLE TX/RX Board, VDD = 3.3 V, Wire-Wound Inductors)

Pout = +10 dBM			
Freq Band	**DDAC[6:0] WW**	**Pout WW (dBm)**	**IDC WW (mA)**
434 MHz	19h	10.4 dBm	16.9 mA
868 MHz	19h	10.3 dBm	16.4 mA
Pout = +13-14 dBm			
Freq Band	**DDAC[6:0] WW**	**Pout WW (dBm)**	**IDC WW (mA)**
434 MHz	3Fh	13.4 dBm	22.7 mA
868 MHz	3Dh	14.3 dBm	24.8 mA
863-921 at 863 MHz	36h	13.3 dBm	24.2 mA
863-921 at 921 MHz	4Ah	13.3 dBm	24.4 mA

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2.1.2. Si4455 CLE for Direct Tie Board Configuration: Component Values and Performance

Table 3 provides the component values required for output power levels of both +10 and +12 to 13 dBm using the Single Antenna with Direct Tie board configuration of Figure 2 and a supply voltage of V_{DD} = 3.3 V. The matchings listed in Table 3 are for wire-wound inductors. Matching network component values are given for multilayer inductors in Table 4. For other frequencies, consult with a Silicon Labs representative.

Table 3. Match Network Component Values vs. Freq
(Direct Tie Si4455 CLE Board, VDD = 3.3 V, Wire-Wound Inductor)

Pout = +10 dBm													
Freq Band	RX Side				TX Side								
	LR1	LR2	CR1	CR2	Lchoke	C0	L0	CM	LM	CM2	LM2	CM3	RDC
434 MHz	56 nH	56 nH	5.1 pF	2.7 pF	220 nH	18 pF	56 nH	8.2 pF	18 nH	15 pF	18 nH	8.2 pF	0 Ω
868-915 MHz	20 nH	24 nH	3 pF	1 pF	120 nH	33 pF	8.2 nH	5.1 pF	6.8 nH	10 pF	6.8 nH	5.1 pF	0 Ω
Pout = +13 dBm													
Freq Band	RX Side				TX Side								
	LR1	LR2	CR1	CR2	Lchoke	C0	L0	CM	LM	CM2	LM2	CM3	RDC
HP 434 MHz	56 nH	56 nH	5.1 pF	2.7 pF	220 nH	10 pF	56 nH	10 pF	18 nH	15 pF	18 nH	8.2 pF	0 Ω
HP 868 MHz	20 nH	24 nH	3 pF	1 pF	120 nH	3.6 pF	19 nH	2.7 pF	9.1 nH	5.1 pF	9.1 nH	2.7 pF	0 Ω

Table 4. Match Network Component Values vs. Freq
(Direct Tie Si4455 CLE Board, VDD= 3.3 V, Multilayer Inductor)

Pout = +10 dBm												
Freq Band	RX Side				TX Side							
	LR1	LR2	CR1	CR2	Lchoke	C0	L0	CM	LM	CM2	LM2	CM3	RDC
315 MHz	82 nH	68 nH	7.5 pF	3.6 pF	270 nH	12 pF	100 nH	10 pF	22 nH	18 pF	22 nH	10 pF	0 Ω
345 MHz	82 nH	68 nH	7.5 pF	3.6 pF	270 nH	15 pF	82 nH	10 pF	22 nH	18 pF	22 nH	10 pF	0 Ω
390 MHz	68 nH	68 nH	5.1 pF	2.4 pF	220 nH	18 pF	68 nH	10 pF	18 nH	18 pF	18 nH	10 pF	0 Ω
434 MHz	56 nH	56 nH	5.1 pF	2.7 pF	220 nH	18 pF	56 nH	8.2 pF	18 nH	15 pF	18 nH	8.2 pF	0 Ω
868-915 MHz	18 nH	22 nH	3 pF	1.2 pF	120 nH	33 pF	8.2 nH	5.1 pF	6.8 nH	10 pF	6.8 nH	5.1 pF	0 Ω
Pout = +13 dBm												
Freq Band	RX Side				TX Side							
	LR1	LR2	CR1	CR2	Lchoke	C0	L0	CM	LM	CM2	LM2	CM3	RDC
HP 434 MHz	56 nH	56 nH	5.1 pF	2.7 pF	220 nH	6.2 pF	56 nH	10 pF	18 nH	15 pF	18 nH	8.2 pF	0 Ω
HP 868 MHz	18 nH	22 nH	3 pF	1.2 pF	120 nH	3.6 pF	18 nH	2.7 pF	9.1 nH	5.1 pF	9.1 nH	2.7 pF	0 Ω

The 169 MHz Class E multilayer DT match has a significantly different structure as shown in Figure 3. The element values are given in Table 5. The value of CC2 is 470 pF. Also, here, the 479 nH Lchoke inductor is a 0603-sized one because this value does not exist in the 0402 size. Currently, the 169 MHz DT match exists with multilayer inductors only.

A summary of typical measured output power, current consumption, and sensitivity in RX mode (100 kbps, H = 1, 0.1% BER) for direct tie board configurations and circuit realizations is shown in Table 5. These results were obtained with a supply voltage of V_{DD} = 3.3 V. The multilayer inductor versions have worse efficiency and sensitivity. In addition, the 13 dBm cannot be achieved on low bands (e.g 434 MHz) with multilayer inductors.

Table 5. Matching Network Component Values at 169 MHz
(Direct Tie Si4455 CLE Board, VDD= 3.3 V, Multilayer Inductor)

Freq Band	RX Side				TX Side												
	LR1	LR2	CR1	CR2	Lchoke	C0	L0	CM	LM	LM2	CM2	LM3	CM3	LM4	CP1	CP2	RDC
169 MHz	220 nH	150 nH	12 pF	6.2 pF	470 nH	39 pF	22 nH	6.8 pF	56 nH	47 nH	18 pF	68 nH	18 pF	47 nH	3 pF	2 pF	0 Ω

Table 6. Output Power, Current Consumption and RX sensitivity vs. Frequency
(Direct Tie Si4455 CLE Board, VDD= 3.3 V, Wire-Wound (WW) and Multilayer (ML) Inductors)

Freq Band	DDAC[6:0] WW	Pout WW (dBm)	IDC WW (mA)	Sens WW (dBm)	DDAC[6:0] ML	Pout ML (dBm)	IDC ML (mA)	Sens ML (dBm)
Pout = +10 dBm								
169 MHz	TBD	TBD	TBD	TBD	23h	10.3 dBm	18.4 mA	-102.8 dBm
315 MHz	TBD	TBD	TBD	TBD	3Fh	10.3 dBm	16.9 mA	-104.5 dBm
345 MHz	TBD	TBD	TBD	TBD	34h	10.2 dBm	17.0 mA	-104.0 dBm
390 MHz	TBD	TBD	TBD	TBD	21h	10.0 dBm	16.8 mA	-104.0 dBm
434 MHz	1Ah	10.2 dBm	16.9 mA	-106.1 dBm	2Ah	10.3 dBm	17.1 mA	-103.1 dBm
868-915M, 868M op.	20h	10.5 dBm	19.7 mA	-104.2 dBm	20h	10.7 dBm	19.7 mA	-103.2 dBm
868-915M, 915M op.	20h	10.5 dBm	19.6 mA	-104.1 dBm	20h	10.3 dBm	19.3 mA	-102.9 dBm
Pout = +12…13 dBm								
HP 434 MHz	3Fh	13.3 dBm	23.0 mA	-105.2 dBm	4Fh	12.3 dBm	23.3 mA	-104.2 dBm
HP 868 MHz	44h	14.3 dBm	25.6 mA	-104.2 dBm	3Ch	13.3 dBm	24.1 mA	-102.0 dBm
868-915M, 868M op.	4Fh	13.7 dBm	25.5 mA	-104.2 dBm	4Fh	13.4 dBm	24.7 mA	-103.3 dBm
868-915M, 915M op.	4Fh	13.3 dBm	24.7 mA	-104.1 dBm	4Fh	12.4 dBm	23.7 mA	-103.3 dBm

At all frequencies, the RX sensitivities achieved with the Direct Tie board configuration are within 2 dB of those obtained with the Split TX/RX board configuration.

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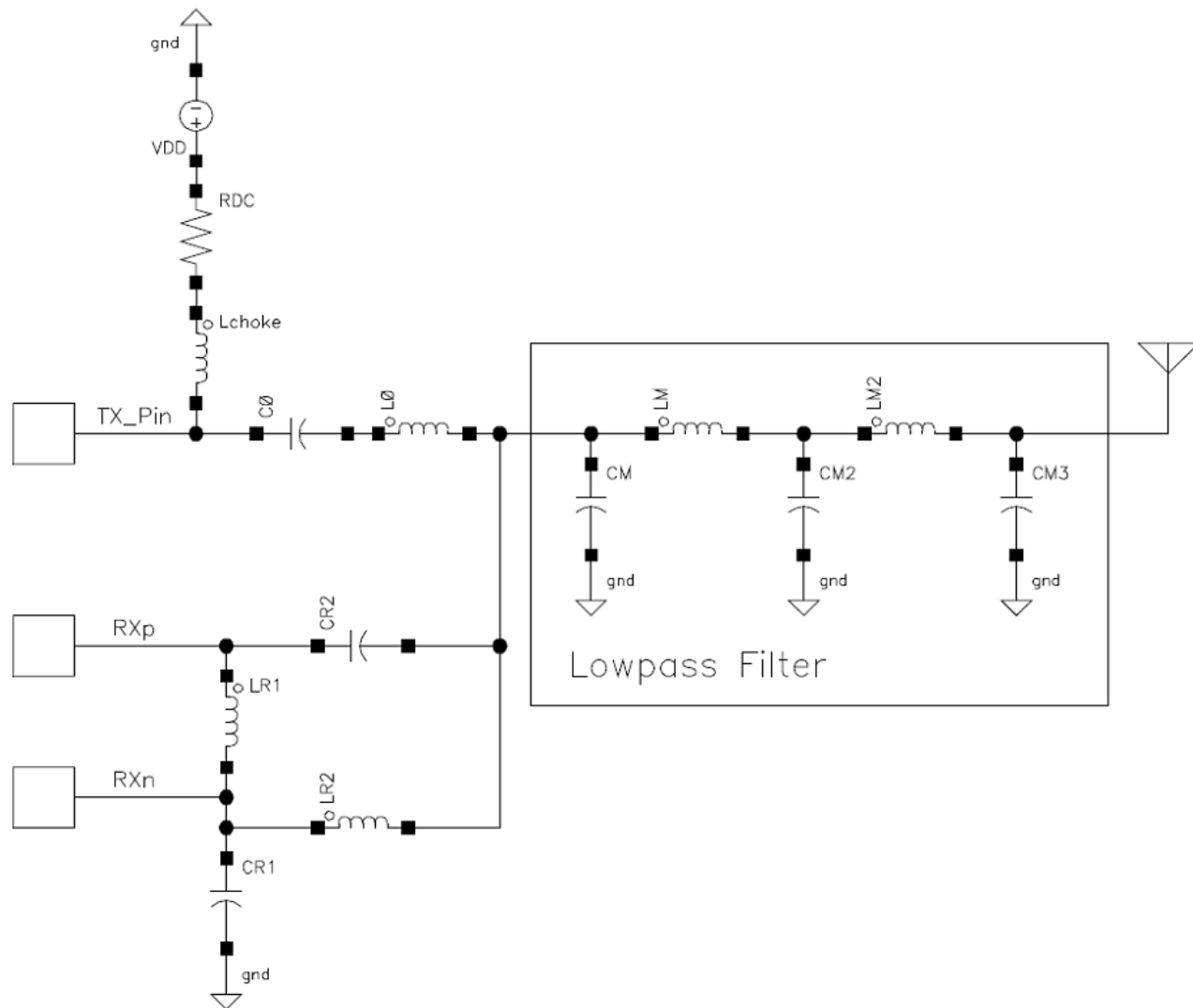
Figure 2. Matching Topology for Single Antenna with Si4455 Direct Tie CLE Board Configuration
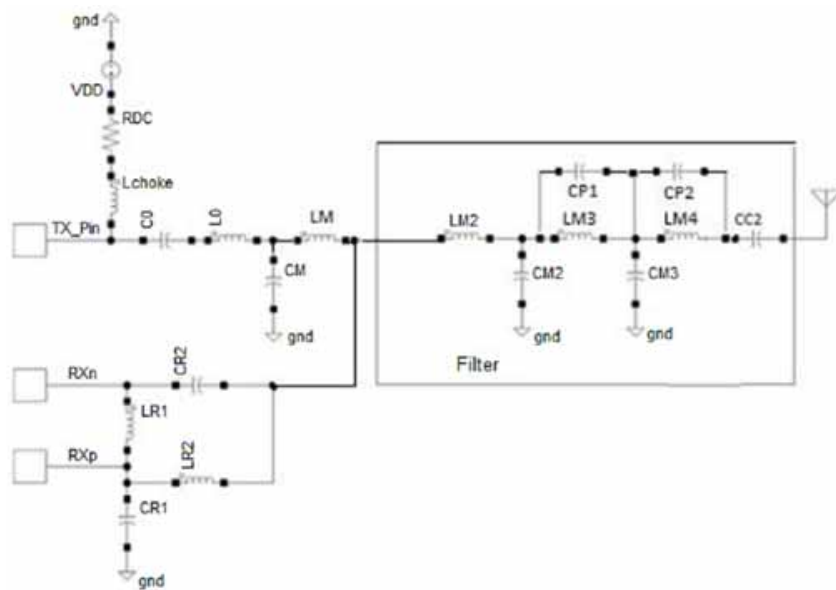
Figure 3. Matching Topology for Single Antenna with Si4455 Direct Tie CLE Board Configuration at 169 MHz

3. Class E (CLE) Matching Procedure Overview

This section provides a description of the Class E type switching mode matching of the power amplifier (PA) on the Si4455 of RFICs.

The maximum peak voltage should be lower than 8 V for long-term reliability.

The Class E matching design flow here is shown on the TX path of a split configuration. The special steps required for DT design (incl. RX path design) are summarized in a separate chapter.

3.1. Brief Overview of CLE Matching Procedure

This application note discusses the CLE matching philosophy and procedure for the Si4455 RFIC in great detail. However, some users may be interested in quickly gaining a high-level overview of the procedure before getting into the fine details. For those readers, the main points of the matching procedure are summarized below:

- Choose L_{CHOKE} (pull-up inductor) for high impedance at Fo.
- Calculate the required value of Z_{LOAD}, given Fo.
- Calculate required PA switcher loss for given V_{DD} and desired output power . In the matchings applied here instead of an external Rdc the necessary loss is introduced by the tuning of the PA switcher FET loss (i.e with the PA power level setting).
- Choose the value for C0 (series capacitor).
- Calculate L0 (series inductor) and required matching component values LX and CX.
- Design a Chebyshev LPF (for attenuation of harmonics).

3.2. Power Amplifier Circuit Description

RF design engineers are familiar with matching conventional (Class A/B/C) power amplifiers. In such cases, the matching procedure is relatively simple: provide a load impedance that is the complex conjugate of the output impedance of the PA. The reader may also employ Load Pull techniques in which a match is found that optimizes the output power but differs from the complex conjugate of the PA output impedance. In these conventional classes of power amplifiers, the output waveform ranges from a full 360 degree copy or reproduction of the driving waveform (e.g., Class A) to a partial (less than 360 degree) reproduction of the driving waveform (e.g., Class B or Class C).

However, the class E type PA circuitry in the EZRadio2 family RFICs differs considerably from such a conventional power amplifier. Specifically, the PA circuitry in the EZRadio2 family is capable of working as a "switching power amplifier" or "switching power converter". The matching procedure for such a class of PA is entirely different and may not be immediately intuitive.

3.3. Basic Switching PA Circuit Topology

At the very heart of a switching PA is a switch. In the Si4455, the switch is provided by group of NMOS transistors. Above the switcher FETs, a cascode stage with open collector output is used to increase the Vpeak allowed at the output. The number of bottom transistors can be tuned and sized to handle the current required for the specified output power.

The Si4455 PA has 79 MOS switching fingers so the DDAC[6:0] field in the PA_PWR_LVL property register can go up to 4Fh. Its typical output capacitance is 1.25 pF independent of the DDAC setting due to its cascode architecture.

Figure 4 shows the basic Class E matching circuitry necessary to extract RF power from a switching amplifier. In very general terms, the value of the pull-up inductor "L_{CHOKE}" is chosen to be a very large impedance at the frequency of operation (and its nearest harmonics), while the series-resonant output tank (L0-C0) is chosen to resonate at the frequency of operation. The shunt capacitance "C_{SHUNT}" is required to store energy during the switching cycle. This shunt capacitance, along with the extra series inductance "LX", also works to tailor the time-domain shape of the output waveform. It is important to understand that, in order to optimize the efficiency of a switching-type amplifier, it is necessary to control the time-domain shape of the output waveform.
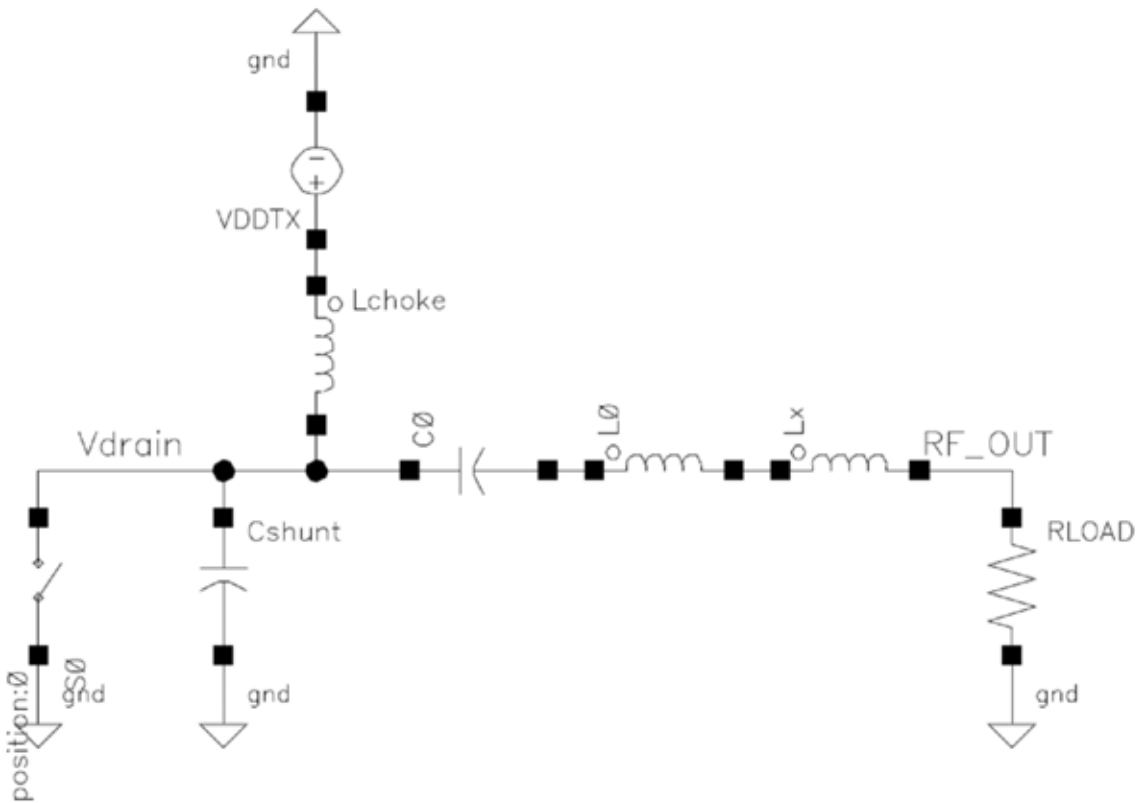
Figure 4. Basic Switching PA Circuit Topology

3.4. Theory of Operation of an Ideal Switching PA

Exactly how does a switch "amplify" an RF signal? The simple answer is that it does not. After all, as long as the input control signal to the switch is sufficient to toggle the switch between its ON and OFF states, the output waveform will remain the same. Thus, the amount of output power delivered to the load resistance is independent of the amplitude of the input control signal (i.e., the amplitude of the RF signal at the gate of the output MOS device) i.e., a switching PA is a strongly nonlinear device. In such a case, defining the "gain" or amplification factor of the PA no longer has much meaning. Technically speaking, it is more correct to refer to this circuit as a "power converter" rather than a "power amplifier".

So, if the circuit does not amplify the internal RF input signal, what determines the level of the output power?

In an ideal class E switching PA, the level of output power is dependent primarily upon two parameters: 1) the dc supply voltage and 2) the shunt capacitance. This statement is actually quite interesting because, theoretically, there is no limit to the amount of power we can extract from a switching PA. Higher levels of output power can be obtained by either increasing the supply voltage or by increasing the shunt capacitance at the switching output device.

Furthermore, in an ideal switching PA, it is theoretically possible to achieve 100% efficiency. This is a significant difference from conventional PAs. It is easily shown that the theoretical maximum efficiency of a Class-A PA is 50%, 78.5% for Class-B, and so on. However, in a switching PA, it is possible to tailor the output waveform such that the voltage across the switch is always zero during any period of time that the switch is conducting current, and the current conducted by the switch is always zero during any period of time that the voltage across the switch is non-zero. Thus, the power dissipated by the switching device itself is zero, and, in the absence of any other losses in the circuit, the efficiency approaches 100%. The theoretical voltage waveform at the drain of a switching amplifier operated in Class-E is shown in Figure 5.
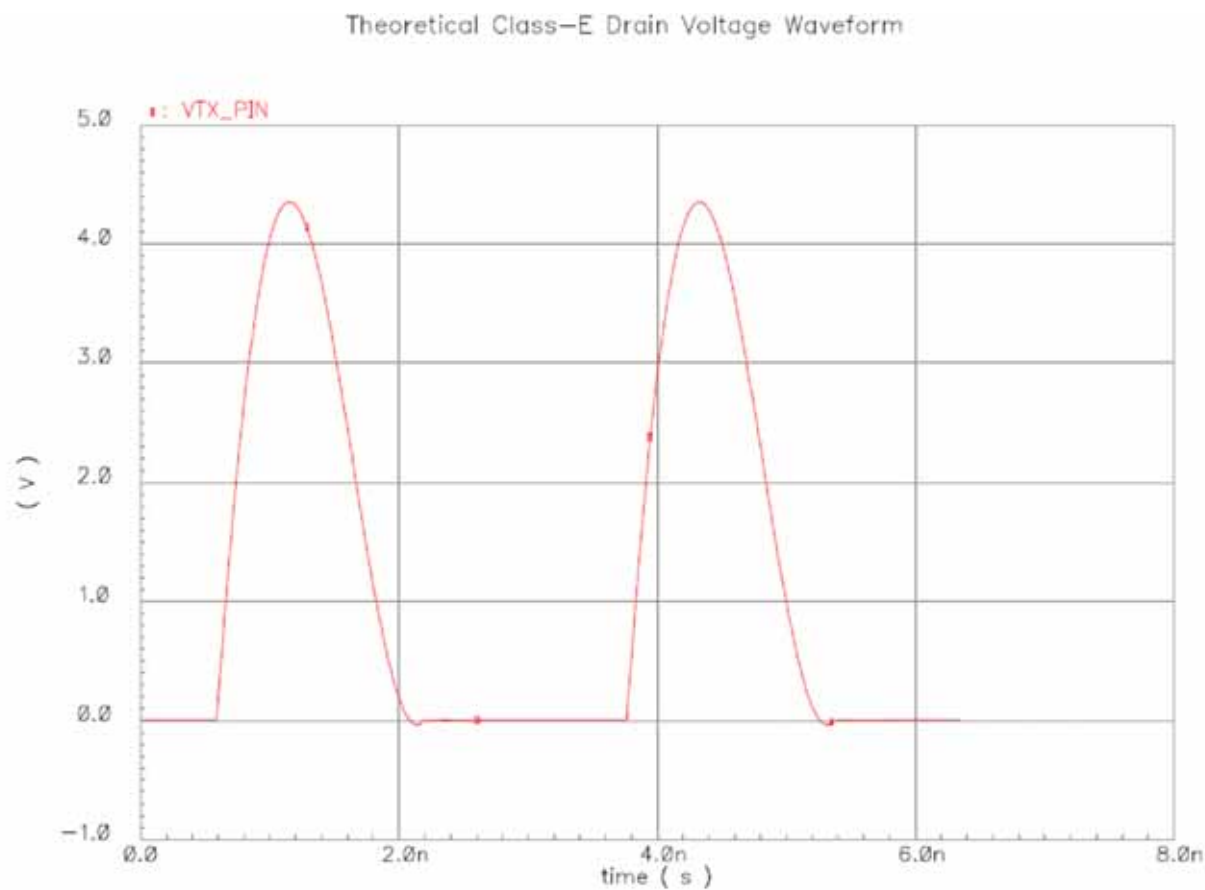
Figure 5. Theoretical Class-E Drain Voltage Waveform

For those interested in learning more about the theoretical operation of switching amplifiers (especially Class-E amplifiers), the following papers are recommended:

- Class E - A New Class of High-Efficiency Tuned Single-Ended Switching Power Amplifiers, N. Sokal and A. Sokal, IEEE Journal of Solid State Circuits, Vol. SC-10, No. 3, June 1975.
- Idealized Operation of the Class-E Tuned Power Amplifier, F. Raab, IEEE Transactions on Circuits and Systems, Vol. CAS-24, No. 12, December 1977.

3.5. Limitations of a Practical MOS Switching PA

In practice, of course, we must live with several factors that prevent us from ever achieving "ideal" operation of the switching PA. These factors include the maximum operating voltage of the switch (i.e., MOS output device), the maximum current (limited by the size of the MOS output device), the ON and OFF state resistances of the MOS output device, non-zero switching times of the MOS output device, and losses in the output matching components due to finite Qs. All of these factors combine to limit the achievable output power and efficiency.

The limitation on the maximum drain voltage of the MOS output device turns out to be a considerable constraint. RF design engineers may be quite familiar with the waveforms obtained with inductively-loaded conventional PAs where the peak output voltage reaches a value equal to twice the dc supply voltage. However, the peak of the output voltage waveform in a switching PA may far exceed this "2xV_{DD}" rule-of-thumb. As is shown in the papers listed above, the peak drain voltage for a Class-E switching amplifier can reach 3.56 x V_{DD}.

The operational range of supply voltage for the Si4455 RFICs is specified as V_{DD} = 1.8 to 3.6 V. It is apparent that, if the switching PA circuit was matched for Class-E operation at V_{DD} = 3.6 V, the resulting peak drain voltage would reach 12.8 V peak. This exceeds the maximum voltage at which the MOS devices can operate reliably without damage (even in cascade configuration). As a result, the drain voltage must be constrained when matching the Si4455 for Class-E operation. This is accomplished by introducing loss. It can be either a suitable choice of a limiting resistor, R_{DC}, in series with L_{CHOKE} or it can be a properly tuned switcher loss. The matching procedure discussed in this application note takes care to constrain the peak drain voltage to a specified maximum value by proper tuning of the switcher loss.

The switching loss here can be modeled as a series resistance, which causes a dc voltage drop on the switcher (i.e., with this loss, the PA supply voltage on the switcher output is decreasing). If the Class E waveform is maintained, the allowed maximum of this PA supply voltage is Vpeakmax/3.56 V = 8 V/3.56 V = 2.24 V as the maximum voltage rating of the semiconductor process for the cascode configuration to have reliable long-term operation is 8 to 8.5 V.

As mentioned earlier, in Class E operation, the output power at a given operating frequency is determined by the PA supply voltage or/and by the shunt capacitance (which basically influences the peak current) at the drain of the switching output device. As in a real amplifier, the PA supply voltage has to be decreased by the loss in order to limit the peak voltage, and the necessary shunt capacitance has to be increased to keep the targeted power; the increased capacitance results in a higher current peak and a higher dc current as well (since the peak current/dc current ratio is fixed ~2.56 in class E operation). That is, a real Class E PA with tuned loss sacrifices efficiency to keep the 8 V peak voltage restriction at higher supply voltage levels.

Moreover, this is the optimum situation, where the PA shunt cap value is adjusted to be close to the 8 V maximum peak limit at the operating frequency with the targeted power.

In actual use, the PA capacitance is usually fixed. Due to this, especially at higher frequencies and lower power applications, the capacitance value is usually greater than the optimum for an 8 V peak. In this case, the peak voltage and thus the effective supply voltage on the switcher are even lower, i.e., higher voltage drop i.e., higher switcher loss i.e., higher power level back off has to be introduced. Moreover, due to the higher capacitance, the current peak and thus the dc current are higher as well, which degrades the efficiency even more. This is the reason why a device with a higher PA capacitance value is not efficient for high-frequency, low-power applications.

On the other hand, a device with too low of a shunt capacitance value cannot achieve the targeted power with the 8 V voltage peak limit. To achieve the target power, a voltage peak higher than 8 V would be necessary. Since it cannot be allowed again, switcher loss has to be introduced. This is the reason why the lower capacitance device (e.g Si4455) cannot exceed the +12 to 13 dBm level at low (315/434 MHz) frequencies even with wire-wound inductors (although at 434 MHz it is very close to that).

The calculation in "4.3.4. Step #4: Estimate the Required PA_PWR_LVL Register Value from the Calculated Value of a Voltage-Limiting Resistor" on page 20 helps to further explain the situation.

The output capacitances and number of fingers of the Si4455 devices are sized in such a way that they can achieve the targeted normal operation power (i.e. 10 dBm) at wide band with a strongly reduced power state at the typical 3.3 V external supply voltage level. Although the RFIC sacrifice efficiency in this way, it is still one of the best on the market at the time of this writing.

On the other hand, the reduced power state has many advantages. It especially improves the robustness of the PA:

- The PA is less sensitive to load impedance variations. This is especially advantageous in battery-powered applications where any excess current increase of the RFIC (even a short one) caused by antenna impedance changes due to environmental condition variations significantly reduces the battery lifetime.

- There is room for power compensation with decreasing external supply voltage level (e.g. battery discharge) by simply increasing the number of switching fingers of the output device (i.e. by decreasing the switcher loss). Since the device has a built-in supply voltage detector, in theory, with a proper external MCU code, it can be adjusted in an automatic way. Silicon Labs calls it an "adaptive power control". Unfortunately, it is usually efficient only in the supply voltage range of 2.2 to 3.6 V.

The PA capacitance of the Si4455 is 1.25 pF. With that, the IC can achieve 13 to 14 dBm at max power state (with the minimum residual loss of the switcher) at 3.3 V V_{DD} at 868 MHz.

At lower frequencies (434/315 MHz), the capacitance value is too low, and, thus, the typical power that the Si4455 can deliver is only 12 to 13 dBm at 3.3 V V_{DD}.

It should be emphasized that the given power values can be measured after the harmonic filter at the output SMA connector. The power at the Class E tank output (before the filter) is approximately 0.5 to 0.8 dB higher than indicated with wire-wound inductors. With multilayer inductors, the power on the SMA suffers an additional 0.5 dB degradation due to the higher losses (especially filter losses).

A good solution to have flat power and efficiency characteristic over a wide frequency range would be to use a tunable internal PA capacitance feature. However, as the power and efficiency achieved still meet the target both at low and high frequencies, the simpler, fixed PA capacitance method is used in the Si4455.

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4. CLE Matching Procedure for the Si4455

Published matching procedures for well-defined classes of operation of switching amplifiers (such as Class-D or Class-E) may lead to operating conditions that exceed the maximum ratings (voltage or current) for the semiconductor process. As a result, we turn to a "customized" matching methodology that satisfies our desire for output power and efficiency while maintaining operation below the maximum voltage and current ratings for the RFIC. Note that this matching methodology is based upon Class-E theory but adds additional steps to aid in constraining the peak drain voltage.

4.1. Goals for the Matching Procedure

The matching methodology for the Si4455 RFIC is aimed at achieving the following simultaneous goals:

- Basically obtain +10 dBm of conducted RF output power even in DT configuration with multilayer inductors. In some bands, the Si4455 can achieve 13 dBm.
- Constrain the peak drain voltage to not exceed +8 V.
- Maximize efficiency on the PA output stage.
- Comply with ETSI and FCC specifications for spurious emissions.

These goals will be met under the following conditions:

- Operation at any frequency in the 315–960 MHz range.
- Antenna load impedance = 50 Ω.
- The chip is commanded to reduced power level mode (PA_PWR_LVL register is typically between 18h and 2Fh).
- Output power is measured at the matching output after the low-pass filter.
- Limitation on peak drain voltage is met for any V_{DD_RF} = 1.8 to 3.6 V.
- Si4455 Output power of +10 dBm is met for V_{DD_RF} = 3.3 V (minimum) with less than 20 mA current or in some bands the power of +13 dBm with less than 25 mA current even with multilayer inductors.

4.1.1. Comments on Peak Drain Voltage Limit

It should be noted that the +8 V peak drain voltage limit referred to above is not the same as the absolute maximum voltage rating at which the device may experience permanent damage. This absolute maximum voltage rating is higher than +12 V on the TX output pin.

Instead, this peak drain voltage limit of +8 V has been calculated as a limit, which, if not exceeded for continuous periods of time, should allow for multiple years of operation without noticeable degradation in output power. That is to say, if the peak drain voltage were to momentarily slightly exceed +8 V, the device would likely not be instantaneously damaged but might suffer a small decrease in long-term reliability.

In all cases, the voltage limit specified by the absolute maximum voltage rating should not intentionally be exceeded (however briefly) because instantaneous damage may occur.

4.1.2. Comments on Achieving the Targeted Output Power

This chapter is largely targeted at applications that require +10 dBm (Si4455). While this level of output power is readily achievable, meeting the other design constraints (e.g., harmonics) requires careful attention to matching component selection and good board layout techniques. That is to say, it is possible to fail through poor design and board layout practices.

4.2. Matching Procedure Overview

4.2.1. Split TX/RX Board Configuration

The following steps provide a broad overview of the matching methodology for the Split TX/RX board configuration. Further details of each step will be provided later. The required design equations are discussed in "4.3. Detailed Matching Procedure for Split TX/RX Board Configuration".

1. First, select a value for the pull-up inductor, L_{CHOKE}, which provides a very large impedance at the frequency of operation (and its nearest harmonics).

2. Choose/calculate values for series-resonant tank L0-C0 such that L0-C0 resonates at Fo.

3. Calculate the required value of Z_{LOAD} given the desired frequency of operation (Fo) and the known shunt drain capacitance of the Si4455 chip (C_{SHUNT} = ~1.25 pF).

4. Estimate the necessary back-off of the power level setting. For this, calculate the required value for a hypothetical voltage-limiting resistor given the desired output power and main chip supply voltage V_{DD_RF}. However, the calculated value is not used as an Rdc in series with L_{CHOKE} but is instead used to estimate the tuned switcher loss.

5. Calculate the values for matching components LX and CX, given the antenna load resistance (e.g., R_{ANT} = 50 Ω) and the calculated value for Z_{LOAD}.

6. Design a low-pass filter to provide sufficient attenuation of harmonic signals.

   a. The unfiltered waveform at the TX output pin will inherently contain high levels of harmonics.

   b. Depending upon the output power level and desired level of harmonic attenuation, a third to fifth order low-pass filter will likely be required.

4.2.2. Single Antenna with Direct Tie Board Configuration

The following steps provide a broad overview of the matching methodology for the Single Antenna with Direct Tie board configuration. Further details of each step will be provided later. The required design equations are discussed in "4.4. Detailed Matching Procedure for Direct Tie Board Configuration" on page 37.

1. The same as the first step in the split match design (see 4.2.1)

2. The same as the second step in the split match design (chapter 4.2.1)

3. The same as the third step in the split match design (chapter 4.2.1)

4. The same as the fourth step in the split match design (chapter 4.2.1)

5. The same as the fifth step in the split match design (chapter 4.2.1)

6. The same as the sixth step in the split match design (chapter 4.2.1).

7. Construct a 4-element match to the differential RXp/RXn input pins, using the methodology outlined in "AN643: Si446x/Si4362 RX LNA Matching".

8. At 868/915 MHz, deliberately mis-tune the calculated value of L0 downwards by approximately 20–30%. At 315/434 MHz, the split L0 values usually work well.

4.3. Detailed Matching Procedure for Split TX/RX Board Configuration

In this section, we provide further detail about each step of the matching procedure for the Split TX/RX board configuration outlined above. We assume a general chip supply voltage of V_{DD_RF} = 3.3 V.

4.3.1. Step #1: Select a Value for L_{CHOKE}

In Step #1, we select an appropriate value for the pull-up inductor, L_{CHOKE}.

In the theoretical derivation for Class-E switching amplifiers, it is desired that the impedance of the pull-up inductor, L_{CHOKE}, be zero at dc and infinite at all other frequencies. This is not achievable in practice; however, a large value of inductance provides a reasonable approximation of this performance. The value of L_{CHOKE} should be chosen such that it provides a high impedance at not only the fundamental operating frequency but also at the first few harmonic frequencies. The inductance value should not be so large as to already be at (or past) parallel self-resonance at the desired operating frequency. The exact inductance value is not critical; however, Silicon Labs recommends the following range of inductance values (assuming 0402-size or 0603-size inductors) as a function of the desired operating frequency:

- 315 MHz: approximately 270 nH to 390 nH
- 470 MHz: approximately 220 nH
- 915 MHz: approximately 100 nH

With these inductance values, the self resonant frequency is at least three times higher than the frequency of operation.

4.3.2. Step #2: Choose/Calculate Values for L0-C0 Series-Resonant Tank

In Step #2, we design the L0-C0 tank to be series-resonant at the desired operating frequency, Fo.

It is self-evident that there are an infinite number of combinations of L0-C0 values that can achieve resonance at a desired frequency. However, certain broad guidelines may be used to select one particular solution of component values.

First, it is desirable that the inductance and capacitance values be neither extremely large nor extremely small. Discrete inductors and capacitors with extremely large values are subject to degrading effects due to self-resonance. Discrete components with extremely small values are subject to greater degrading effects due to component tolerances. In either case, the actual resonant frequency of the tank may be significantly different than the frequency predicted by mathematical calculations.

Second, in the theoretical derivation for Class-E switching amplifiers it is desired that the impedance of the L0-C0 series-resonant tank be zero at Fo and infinite at all other frequencies. This is not achievable in practice; however, a reasonable approximation to this performance may be obtained by using values with a high L-to-C ratio.

Third, it is desirable to minimize the insertion loss of the resonant tank. Since the quality factor (Q) of discrete inductors is generally much lower than that of discrete capacitors, it is important to select an L0-C0 ratio that maximizes the inductor Q. The Q of discrete inductors generally increases as the inductance value is also increased until the inductance approaches the value where self-resonance becomes a concern.

Finally, it is desirable to select component values that are near standard 5% tolerance values. Unfortunately, it is rare for multilayer inductors.

These considerations lead to the following guidelines for selecting the values for L0-C0:

- The L0-C0 tank must resonate at Fo.
- The value of L0 should be chosen as large as possible
- While remaining low enough that the effects of self-resonance are not an issue
- And are close to standard 5% tolerance values

In the present 868M design, we choose 3.6 pF as C0 and 9.3 nH as an L0 value.

4.3.3. Step #3: Calculate the Required Value for Z_{LOAD}

In Step #3, we calculate the required value of load impedance to be presented to the output of the L0-C0 resonant tank, at the fundamental operating frequency, Fo.

In the theoretical derivation for Class-E switching amplifiers, it may be shown that the equations for output power (P_{OUT}) and load impedance (Z_{LOAD}) as a function of shunt drain capacitance (C_{SHUNT}) and supply voltage (V_{DD}) are as follows:

$$P_{OUT} = \pi\omega_o C_{SHUNT} V_{DD}^2$$

Equation 1.

$$Z_{LOAD(fund)} = \left(\frac{0.2815}{\omega_o C_{SHUNT}}\right) e^{j \times 49.0524°}$$

Equation 2.

These two equations are quite interesting. Equation 1 states that the theoretical output power is not a function of load impedance, but instead depends only upon the shunt drain capacitance (C_{SHUNT}), the desired operating frequency ($\omega_o = 2\pi Fo$), and the PA supply voltage (V_{DD}).

$$R_{OUT} = \left(\frac{G_{OUT}}{G_{OUT}^2 + B_{OUT}^2}\right)$$

Equation 2 states that the required load impedance (Z_{LOAD}) does not vary with the desired level of output power, but depends only on the desired operating frequency and value of shunt drain capacitance.

The value of shunt drain capacitance, C_{SHUNT}, is a design parameter of the Si4455 RFIC and is not adjustable by the user. This shunt capacitance is composed primarily of the drain-source capacitance (Cds) of the output MOS cascade devices in parallel with a small amount of explicit integrated capacitance. Silicon Labs states that the value of this shunt drain capacitance is approximately:

- C_{SHUNT} = 1.25 pF for Si4455

These values may be substituted in the equations above and used to calculate other matching parameters. Assuming a desired operating frequency of Fo = 868 MHz as an example, the following value for Z_{LOAD} may be calculated for Si4455:

$$Z_{LOAD(315M)} = \left(\frac{0.2815}{2\pi \times 868M \times 1.25\text{ pF}}\right) e^{j \times 49.0524°} = 27.06 + j31.18\,\Omega$$

Equation 3.

This is the value of load impedance (at the fundamental operating frequency) that must be presented to the output of the L0-C0 resonant circuit.

It should be clearly understood that the value of load impedance (Z_{LOAD}) discussed above and the antenna impedance (Z_{ANT}) are not the same parameter, nor do they necessarily have the same ohmic value. Given the arbitrary impedance of the antenna, the next task will be to construct a matching network that transforms Z_{ANT} into Z_{LOAD}, as seen at the output of the L0-C0 resonant circuit.

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4.3.4. Step #4: Estimate the Required PA_PWR_LVL Register Value from the Calculated Value of a Voltage-Limiting Resistor

In Step #4, we estimate the necessary power backoff i.e., the DDAC field value of the PA_PWR_LVL register required for the desired output power. For this, the calculation of a hypothetical voltage-limiting resistor (not used directly in the circuit as RDC) is required for a given specified value of PA supply voltage (V_{DD}).

Equation 1 clearly shows that, for a given desired operating frequency, the only "knob" remaining to the user to select the output power is the PA supply voltage, V_{DD}, since the value of C_{SHUNT} is an internal chip design parameter and is not adjustable by the user. Equation 1 is easily solved for V_{DD} and is found to be:

$$V_{DD} = \sqrt{\frac{P_{OUT}}{\pi \omega_o C_{SHUNT}}}$$

Equation 4.

Continuing our design example at 868 MHz and assuming a desired output power of +13.7 dBm (~23.4 mW) to compensate the losses and get ~13 dBm after filtering, the required value of V_{DD} may be calculated as:

$$V_{DD} = \sqrt{\frac{0.0234}{2\pi^2 \times 868M \times 1.25pF}} = 1.045 \text{ V}$$

Equation 5.

This equation states that if the voltage supplied to the top of pull-up inductor L_{CHOKE} is equal to 1.045 V and the previously-calculated value of load impedance Z_{LOAD} is presented to the chip, the resulting output power will be P_{OUT} = 23.4 mW = +13.7 dBm at the class E tank output in an ideal loss-free case.

This required PA supply voltage (V_{DD}) is significantly different from the general supply voltage (V_{DD_RF}) for the rest of the RFIC. It is obviously not desirable to maintain two separate, independent sources of supply voltage for the RFIC; therefore, it is convenient to create the PA output supply voltage from the main supply voltage by means of an I-R voltage drop across a resistor.

This resistor can be either a series external resistor with L_{CHOKE} (R_{DC}) or an internal switcher loss. As the theoretical efficiency of an ideal Class-E switching amplifier tank is 100%, the average drain current I_{DD} may be calculated as:

$$P_{OUT} = \pi \omega_o C_{SHUNT} V_{DD}^2 = I_{DD} V_{DD}$$

Equation 6.

This equation may be solved for I_{DD} to obtain:

$$I_{DD} = \pi \omega_o C_{SHUNT} V_{DD}$$

Equation 7.

Given the main supply voltage for the remainder of the chip (V_{DD_RF}) and having previously calculated the required value of PA supply voltage (V_{DD}) and average drain current ($I\overline{D}D$), it is a simple matter to calculate the required value for RDC:

$$R_{DC} = \frac{V_{DD\_RF} - V_{DD}}{I_{DD}}$$

Equation 8.

Continuing our design example at 868 MHz for +13.7 dBm Class E tank output power, we calculate:

$$I_{DD} = 2\pi^2 \times 868M \times 1.25 \text{ pF} \times 1.045 \text{ V} = 22.4 \text{ mA}$$

Equation 9.

Assuming a general chip supply voltage of V_{DD_RF} = 3.3 V, we calculate:

$$R_{DC} = \frac{3.3 - 1.045}{0.0224} = 100.7 \ \Omega$$

Equation 10.

Theoretically, this value of resistance must be placed in series with L_{CHOKE} (if it is loss-free) in order to drop the general chip supply voltage down to the value required to obtain the desired output power. In actual use, due to the losses (L_{CHOKE} has significant losses on the order of 10 to 15 Ω, other component losses, etc.) at the operating frequency, the required resistance value is lower.

This power is achieved at an Si4455 DDAC field (of the PA_PWR_LVL register) value of ~34h with wire-wound inductors at 3.3 V. At this power setting, the switcher loss is approximately ~88 Ω; so, together with the other losses, it is a realistic value.

4.3.5. Calculate the Values for Matching Components LX and CX

In Step #5, we calculate the values of the matching components required to transform the given antenna impedance (Z_{ANT}) into the required load impedance (Z_{LOAD}).

This matching effort may be accomplished by conventional design methods, such as the use of a Smith Chart or impedance matching CAD software (e.g., WinSmith™). Continuing our design example at 868 MHz and assuming an antenna impedance of $Z_{ANT} = R_{ANT} = 50\ \Omega$, we find that 50 Ω may be transformed to the required value of $Z_{LOAD} = 27.1 + j\ 31.2\ \Omega$ by shunt matching capacitance $C_X = 3.39$ pF and series matching inductance $L_X = 10.26$ nH. The resulting circuit topology is shown in Figure 10.

It should be noted that this is only one possible solution for the required impedance transformation; other matching topologies could have been used as well. The reader should also note that the required L_X-C_X match topology depends upon the real part of the load impedance, $\text{Re}(Z_{LOAD})$. In this example, the real part of the load impedance was less than 50 Ω and thus an appropriate matching topology consisted of a shunt capacitor (C_X) and a series inductor (L_X). In the event that $\text{Re}(Z_{LOAD})$ had been greater than 50 Ω, an appropriate matching topology would have consisted of first a series inductor (LX) followed by a shunt capacitor (C_X).

It is apparent that series inductors L_0 and L_X in Figure 6 may be combined into one equivalent inductor with a value equal to the sum of their individual inductances in order to reduce parts count. This is a normal and usual practice.
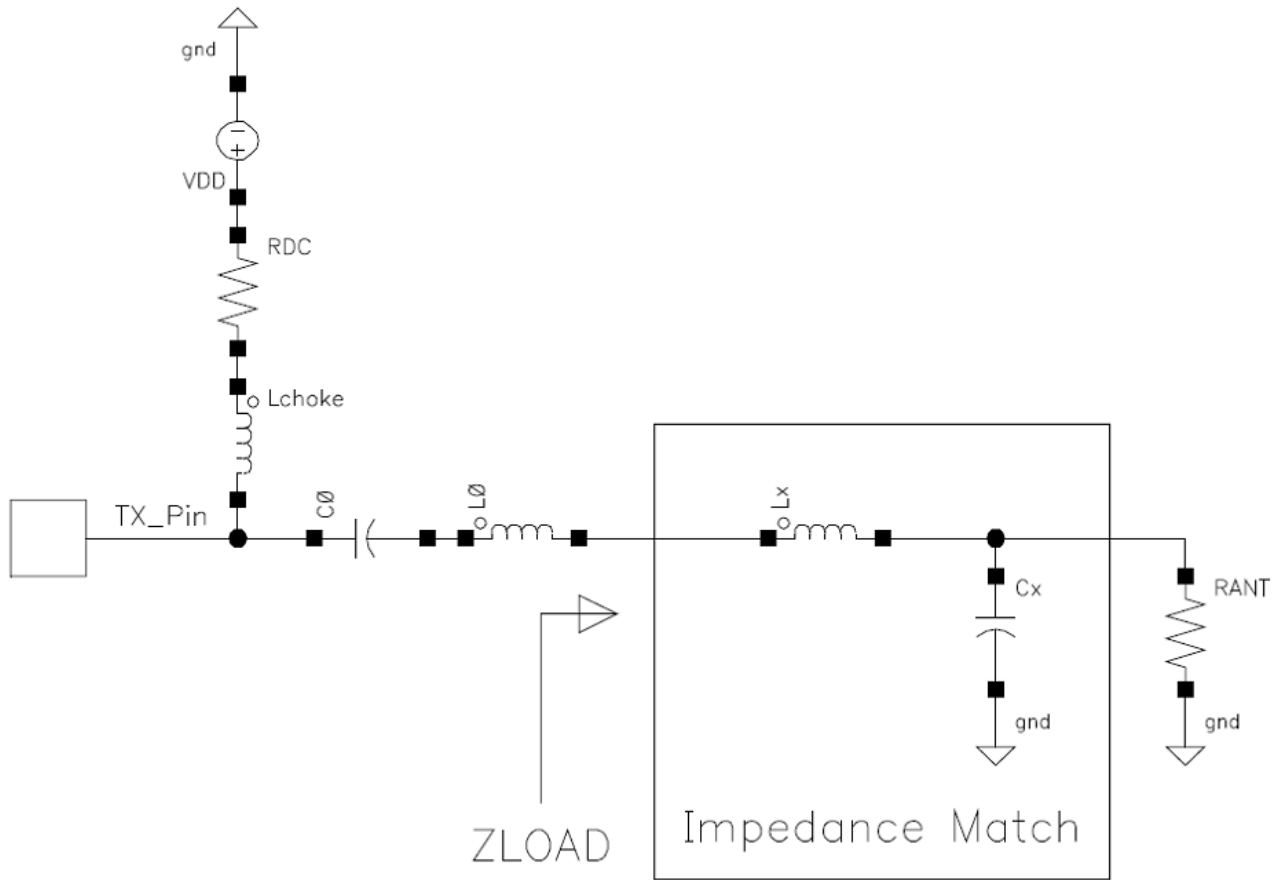
Figure 6. Impedance Match to Transform R_{ANT} to Z_{LOAD}

4.3.5.1. Voltage Waveforms at TX Output Pin

At this point, the basic PA output match is complete. Although we have not yet designed a low-pass filter to sufficiently attenuate the harmonic signals, it is possible to measure the output power by substituting a power meter or spectrum analyzer in place of the antenna impedance (R_{ANT}).

It was previously mentioned that the peak of the drain voltage waveform in a Class-E switching amplifier may reach levels of V_{PEAK} = 3.56 x V_{DD}. (This statement was offered without proof; for those readers interested in the derivation, refer to the papers listed in "3.4. Theory of Operation of an Ideal Switching PA" on page 13.) It is desirable to measure the actual drain voltage waveform in order to ensure compliance with our stated design goal of constraining the peak drain voltage to less than 8 Vpk.

It is not difficult to verify the resulting voltage waveform at the TX output pin (at least for the lower frequency bands of operation). A high-speed oscilloscope with an input bandwidth of at least 4 GHz (preferably higher) is required. A low-capacitance, high-bandwidth scope probe is also required, or, alternatively, the "resistive-sniffing" network of Figure 7 may be used. In this schematic, it can be seen that the inductors L_0 and L_X have been combined into one equivalent series inductance.
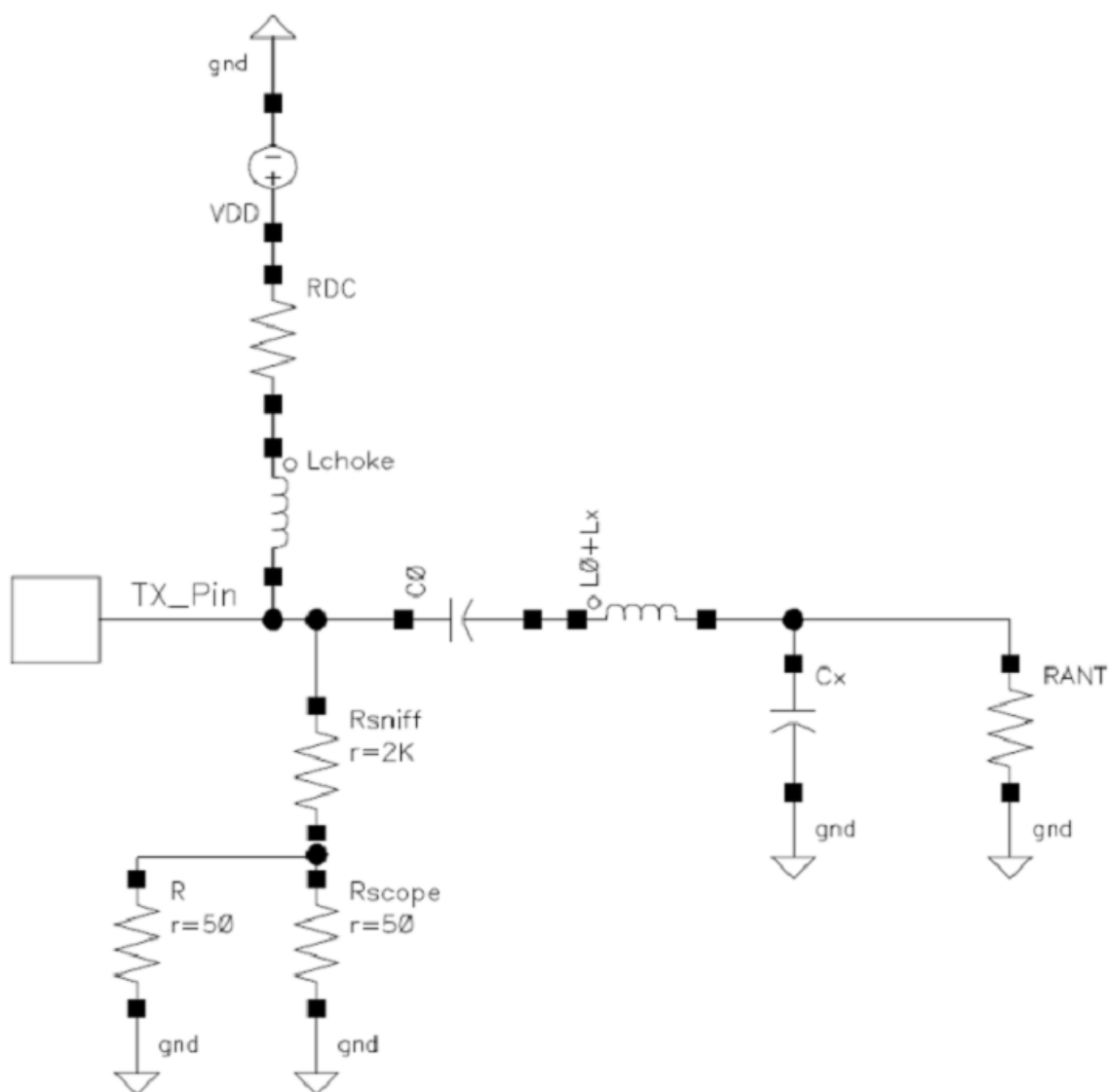
Figure 7. Resistive Sniffing Network

Using the "resistor sniffing" technique of Figure 7, the drain voltage waveform of Figure 8 was observed for an operating frequency of Fo = 868 MHz. In the example shown here, the following component values (obtained through use of the design equations above) were used:

- $P_{OUT(TARGET)}$ = +13.7 dBm
- V_{DD_RF} = 3.2 V
- C_{SHUNT} = 1.25 pF (Si4455)
- L_{CHOKE} = 100 nH
- R_{DC} = 0 Ω
- DDAC value is 35h
- C_0 = 3.6 pF
- $L_0 + L_X$ = ~19 nH
- C_X = 3.3 pF

The measured output power was +13.7 dBm at power state 35h at 3.2 V. The power state 35h required for the targeted power corresponds to approximately 86 Ω switcher on state loss. Together with the dc resistance of the L_{CHOKE}, it is approximately 88 Ω; so, the introduced loss is slightly lower than what is calculated by Equation 10. This is because the design equations above assume ideal switching operation of the output devices (i.e., zero ON-state resistance, infinite OFF-state resistance, zero switching time, etc.) as well as lossless discrete matching components. A practical switching amplifier and output match will inherently fall short of such ideal operation; some small degradation in output power is to be expected, which has to be compensated for by a slight increase of the PA power level setting (i.e further decrease of switcher on-state impedance). In any case, the difference is not significant.
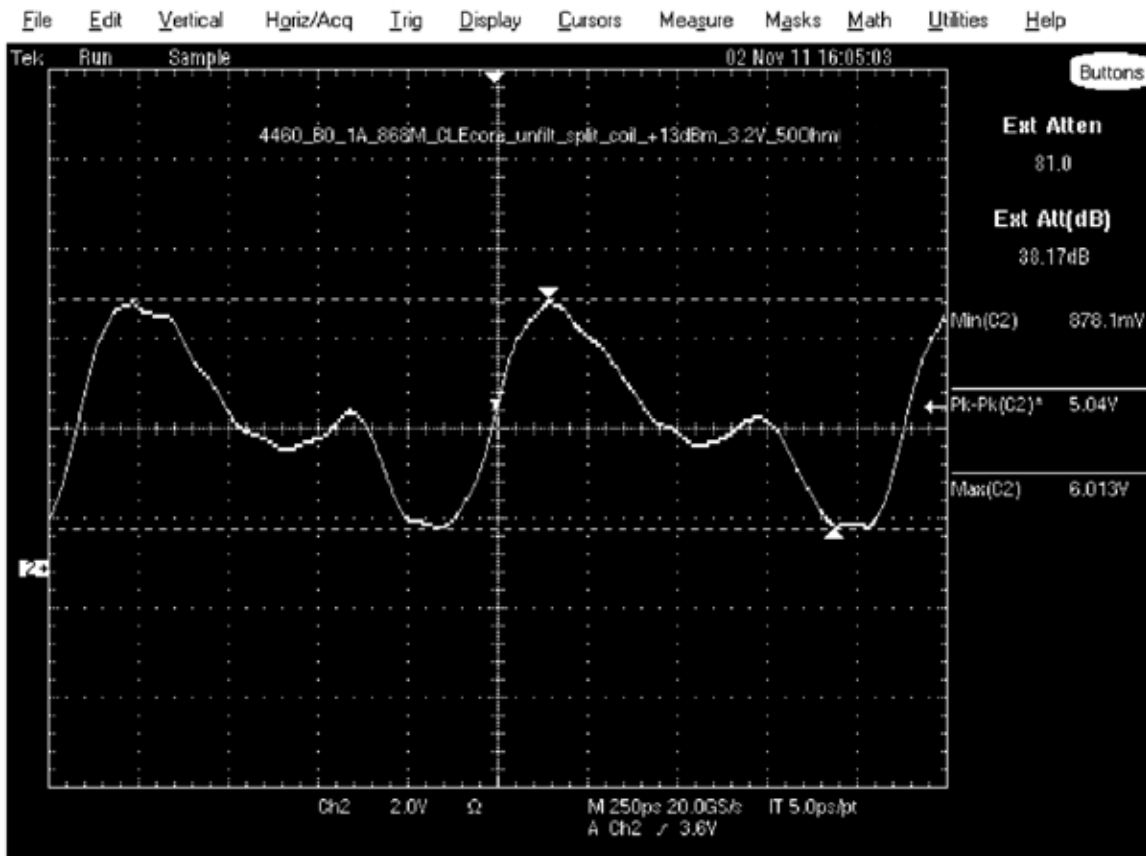
Figure 8. Drain Voltage Waveform (Fo = 868 MHz)

As can be seen in Figure 8, the measured waveform deviates to some extent from the theoretical "Class-E like" waveform at this higher (868 MHz) frequency, but the maximum drain voltage is 6 V, much less than the critical 8 V.

It should be noted that the waveform would be closer to the theoretical Class E waveform at lower (315/868M) frequencies, as shown in Figure 9. As the operating frequency increases, it also becomes more difficult to faithfully observe the waveform. The input bandwidth of the oscilloscope used to display the waveform must increase in accordance with the operating frequency. Additionally, parasitic capacitances of the sniffing system and/or in the PCB layout, as well as in the output device(s) of the RFIC, tend to limit the high-frequency response of the amplifier.
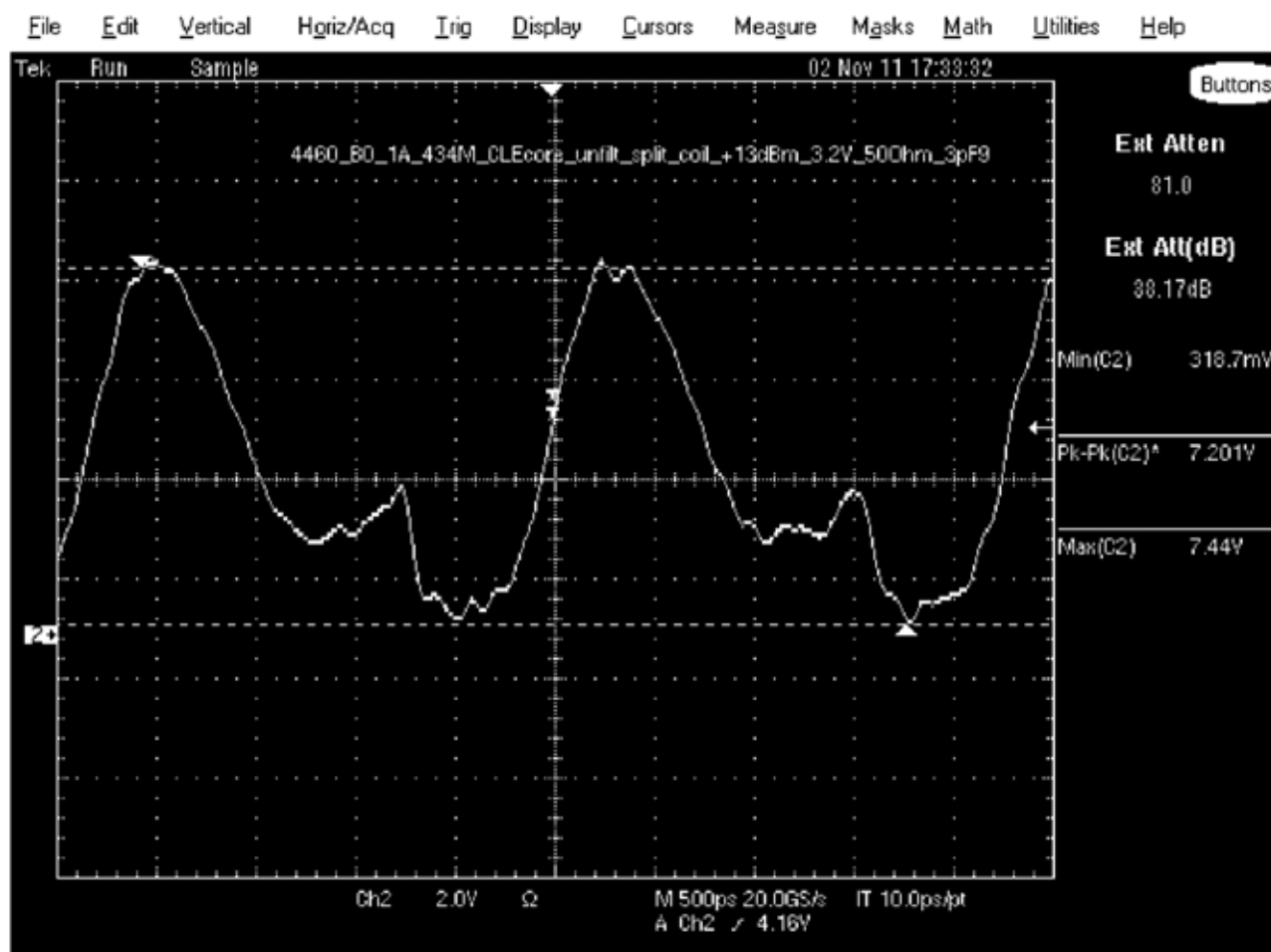
Figure 9. Drain Voltage Waveform of a 434 MHz Class E Tank

4.3.6. Step #6: Design a Low-Pass Filter

In Step #6, we design a low-pass filter network to attenuate the harmonics below the level required to meet applicable regulatory standards, such as FCC or ETSI.

4.3.6.1. Unfiltered Harmonic Spectrum

It should be understood that the waveform at the output of the match shown in Figure 8 will still contain relatively high levels of harmonics. Although the bandpass response of the series-resonant L0-C0 tank provides some attenuation of harmonic signals, it is generally not sufficient to meet applicable regulatory standards. This is normal for such a switching-amplifier and matching topology.

By way of example, the harmonic spectrum at the antenna load (R_{ANT}) for the matching network and component values of Figure 8 is shown in Figure 10 at power state 35h with 25.4 mA total current consumption at 3.2 V.
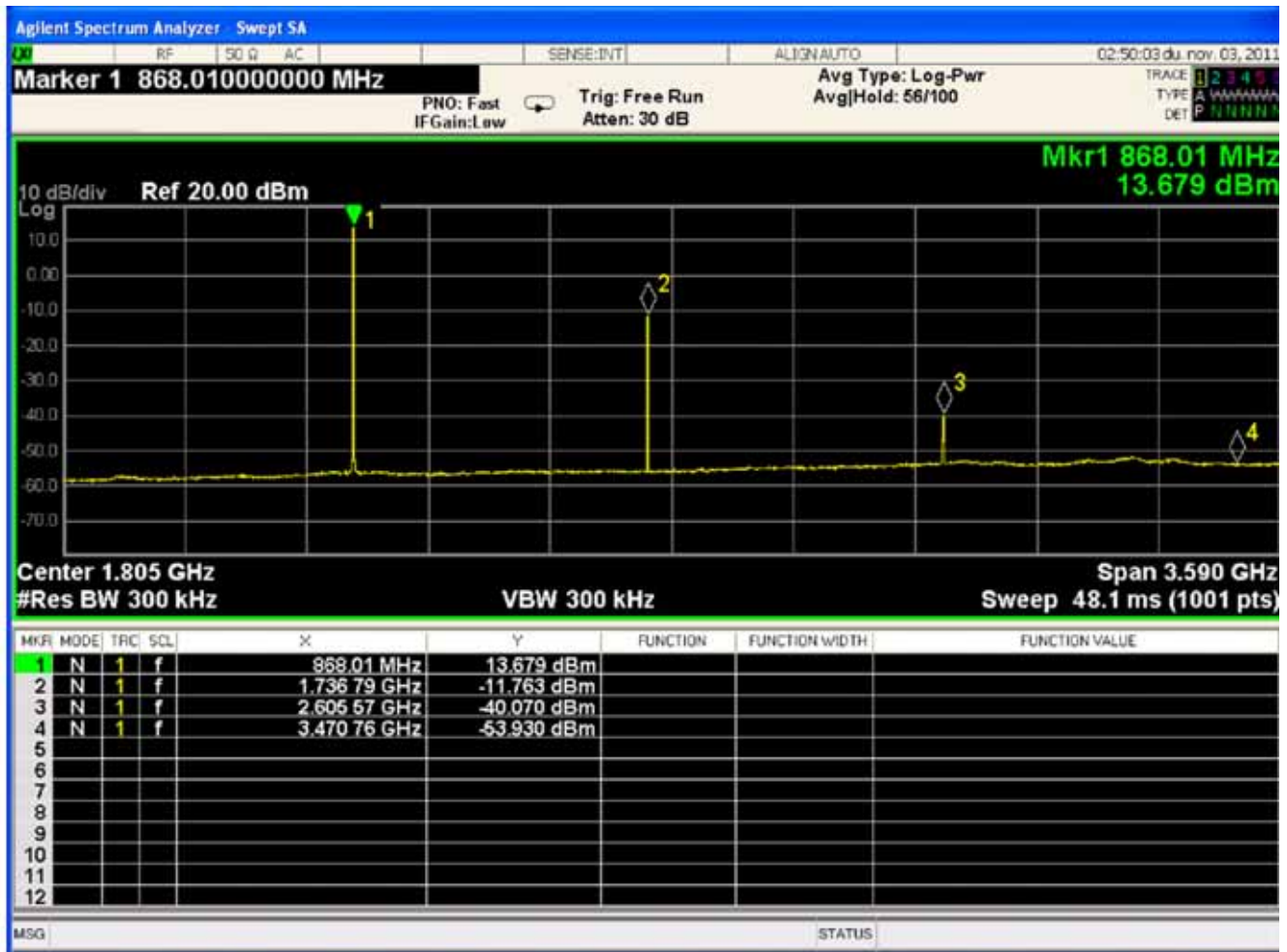
Figure 10. Unfiltered Harmonic Spectrum at Power State 35h at 3.2 V
(Fo = 868 MHz, 25.4 mA Total Current)

It should be noted that this Class E tank uses mainly the calculated values, assuming an ideal loss and parasitic-free case. As mentioned earlier, in a real case, there are losses, non-ideal switching characteristics, and several other parasitics, which degrades the operation with the calculated ideal values. Due to this, some bench tuning is usually useful to improve the performance. Although its mechanism is not fully clarified yet, a typical way to improve efficiency is to decrease the value of CM. For strongly reduced power (10 dBm Si4455 design), the increase of C0 may also improve the efficiency. The following sections describe the final design with filtering.

4.3.6.2. Filtering Requirements

It is difficult for Silicon Labs to recommend one single low-pass filter design that is appropriate for all customers because customers may operate under widely differing regulatory standards, each with different harmonic requirements. However, a common regulatory standard that may be applicable to our design example at 868 MHz is ETSI Part EN300 220. This standard specifies the permitted levels of fundamental and harmonics in terms of Effective Radiated Power (ERP). The 868 MHz ETSI frequency band comprises several subbands with different properties. For example, the allowed power varies between +7 and +27 dBm with most cases at 14 dBm ERP. At our desired operating frequency of 868.3 MHz (G1 subband), these maximum permitted ERP levels are:

- Fundamental = +14 dBm ERP
- Harmonics = –30 dBm ERP

Since the limits are specified in terms of ERP, compliance must be verified by measuring in an anechoic chamber with the unit operated into its intended antenna. The ERP is the power required to the input of an ideal dipole antenna with a gain of 2.14 dB to generate the same electric field at the far field. However, if an ideal isotropic antenna is assumed with 0 dB gain, higher conducted power is required at the antenna input by 2.14 dB. This equivalent level of conducted power is known as Equivalent Isotropic Radiated Power or EIRP.

Using EIRP limits, the equivalent conducted power ETSI limits are slightly higher:

- Fundamental = +16.14 dBm EIRP
- Harmonics = –28.86 dBm EIRP

As can be seen, our targeted +13 dBm power level with Si4455 is approximately 3 dB lower than the fundamental 868M EIRP limit of the ETSI; so, in theory, the gain of the applied antenna can go up to 3 dB. Unfortunately, in real applications, the typical monopole antenna gain is –5 to +2 dB depending on many circumstances, such as available space, circuit dimensions (working as an electrical mirror ground plane), case etc.; so, in most cases, the ETSI fundamental limit is not approached.

However, the same antenna can become a good radiator at the harmonic frequencies, where the antenna's relative size is longer and the same circuit (ground plane) dimensions give better electrical mirror properties i.e., better radiation. It is especially true if the strongly varying antenna impedance with frequency causes acceptable reflection levels at these harmonic frequencies.

Anyway, most of the antenna properties strongly depend on the actual antenna design and are difficult to predict in advance. Because of this, to have margin for a possible worst-case scenario, Silicon Labs usually defines the conducted harmonic levels to be 5 to 6 dB lower than the ERP limit, i.e., for 868 MHz fundamental frequency, they are ~–36 dBm.

4.3.6.3. Selecting an LPF Order and Type

Therefore, given the unknown radiation efficiency of each possible antenna selected by a user, it is difficult for Silicon Labs to conclusively state the required filter attenuation characteristics. As a reasonable design compromise, we settle upon the following design goals for the low-pass filter:

- Minimal insertion loss at the desired operating frequency
- A minimum conducted level of –36 dBm at all harmonic frequencies. Since the most critical second harmonic level is approx –8 to –10 dBm without filtering, the necessary minimum harmonic attenuation is approximately 28 dB.
- Lowest filter order possible to still achieve this required harmonic attenuation
- 1:1 impedance transformation (i.e., 50 input and 50 output impedance)

Note that the amplitude characteristics in the lower portion of the passband of the LPF are relatively unimportant. Because the output signal contains no frequency components below the fundamental frequency, the frequency response of the filter below the desired operating frequency is also of little consequence. We are free to choose the filter type (e.g., Butterworth, Chebyshev, Elliptic) based primarily upon the filter's attenuation characteristics rather than its passband response.

A Butterworth filter design is not optimal because it provides relatively poor high-frequency attenuation characteristics; there is no need to sacrifice high-frequency attenuation in order to obtain a maximally-flat in-band frequency response.

Similarly, an Elliptic filter design (Cauer-Chebyshev) may provide insufficient attenuation at higher-order harmonic frequencies. While it may be possible (and advantageous) to tune a transmission zero in the stopband to the frequency of a problematic harmonic (e.g. N = 2 or N = 3), it is paid for with a decrease in attenuation at higher harmonic frequencies. As the unfiltered harmonic spectrum of Figure 10 shows, there remain several higher-order harmonics with significant energy that cannot be ignored and must be attenuated.

As a result, we settle on a Chebyshev low-pass filter design as an acceptable type of filter response.

With a Chebyshev filter, it is possible to obtain a greater rate of attenuation roll-off in the stopband by accepting a larger amount of amplitude ripple in the passband. The next issue to be addressed is the amount of passband ripple to be targeted in the filter design.

Greater attenuation at high frequencies can be obtained by employing a filter designed for a relatively large amount of passband ripple, but this trade-off should not be pushed too far. While a reasonable amount of passband ripple is perfectly acceptable, there is a limit to what can be considered reasonable.

Figure 11 shows the passband frequency response of an ideal (lossless) Chebyshev filter with 0.17 dB of amplitude ripple in the passband. It is quickly apparent that, in order to minimize the insertion loss of the filter at the desired operating frequency, it is necessary to design the cutoff frequency of the filter such that the desired operating frequency falls at one of the passband amplitude ripple peaks (Cursor "A" in the plot). If the filter cutoff frequency varies due to component tolerances, the filter response may vary such that the desired operating frequency falls on a minimum of the amplitude ripple response rather than on a maximum. In such a scenario, the filter insertion loss will increase, and the TX output power will decrease.

By designing for a limited amount of passband amplitude ripple, an upper limit is placed on the filter insertion loss due to mistuning of the component values. It is the opinion of Silicon Labs that a Chebyshev passband amplitude ripple of 0.15 to 0.5 dB represents a reasonable design trade-off between high-frequency stopband attenuation and potential passband filter insertion loss due to component tolerance.

As mentioned earlier, at 868 MHz, the filter attenuation should be at least 26 dB at the second harmonic frequency. To achieve this, at least a five-order filter is required with the targeted ripple level. Since the cost of an SMD capacitor is usually much lower than that of an SMD inductor (even they are multilayer ones), it is advantageous to choose a filter structure where the filter starts with a parallel capacitance (PI topology).

As usual, the SMD inductors, especially the multilayer ones, have much lower Qs than the SMD capacitors. The smaller number of series inductors is also advantageous because the extra attenuation caused by losses is lower.

S21[dB] Ideal 5th order Chebyshev response with 20% passband reflection and 908.6M cuttoff
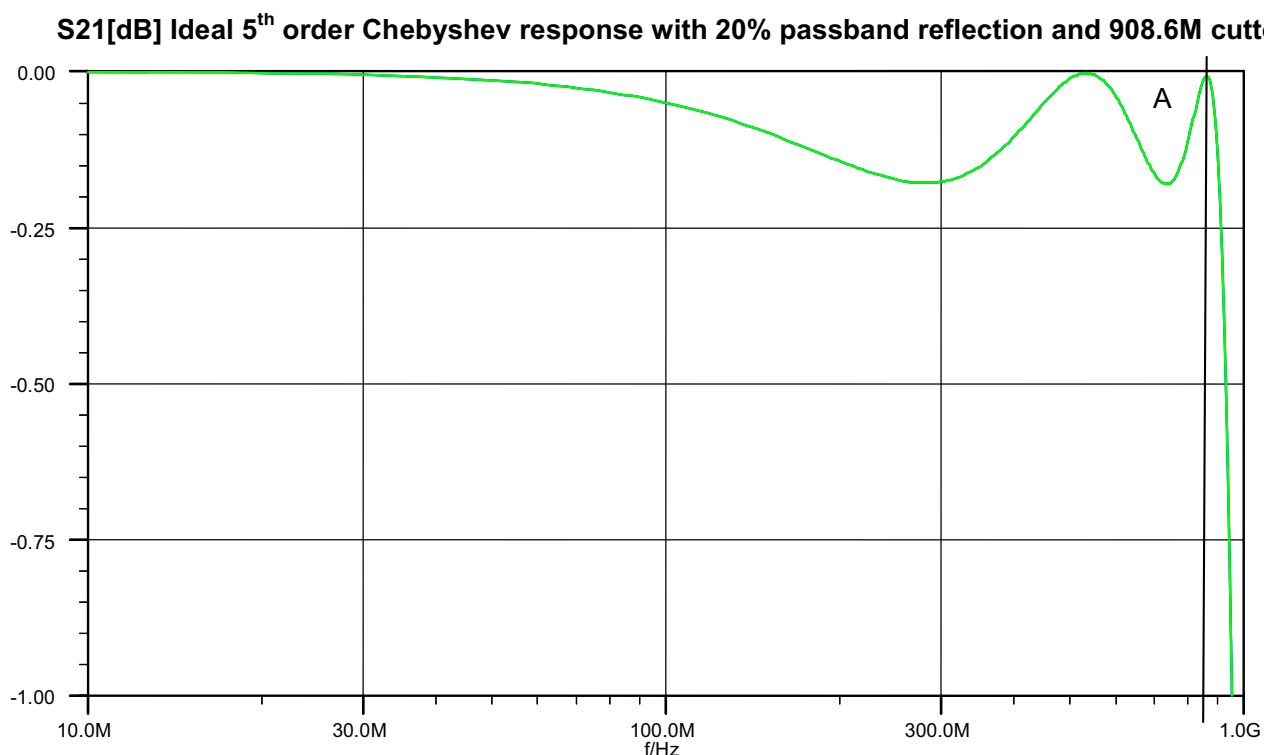
Figure 11. Ideal 5th-Order 0.17 dB Ideal Chebyshev Filter Response at 868 MHz

4.3.6.4. Calculation/Design of Component Filter Values

Actual filter component values may be obtained by the usual design methods, such as the use of Filter Design CAD software or tables of normalized filter values scaled to the desired frequency of operation.

Due to the attenuation margin of the fifth-order design and the extra loss introduced by the losses, here, a slightly lower ripple prototype is chosen: T520 i.e., the maximum passband voltage reflection is 20%, which corresponds to approximately 0.17 dB ripple in a loss-free case.

The possibility of a fourth-order filter was also investigated, but, with that, the highest attenuation at the second harmonic is around 28 to 29 dB, i.e., at the edge without parasitic losses. In order to have margin and also decrease the insertion loss (i.e., to achieve better attenuation with lower passband loss) the fifth order filter was chosen. Moreover, the fifth-order filter uses only one more capacitor, which is a very low-cost element.

Note that Silicon Labs recommends designing the filter such that the desired operating frequency falls at a peak of the amplitude ripple response rather than at the 3 dB cutoff frequency or at the equal amplitude ripple cutoff frequency (F_{ERCUT}). In this manner, the insertion loss of the filter will be minimized, and the TX output power will be maximized. For a fifth-order 0.17 dB Chebyshev filter, the ratio of $F_{ERCUT:FPEAK}$ is approximately 1.0468:1. That is, if the desired operating frequency is 868 MHz, the filter must be designed for an F_{ERCUT} of 315 x 1.0468 = 908.6 MHz.
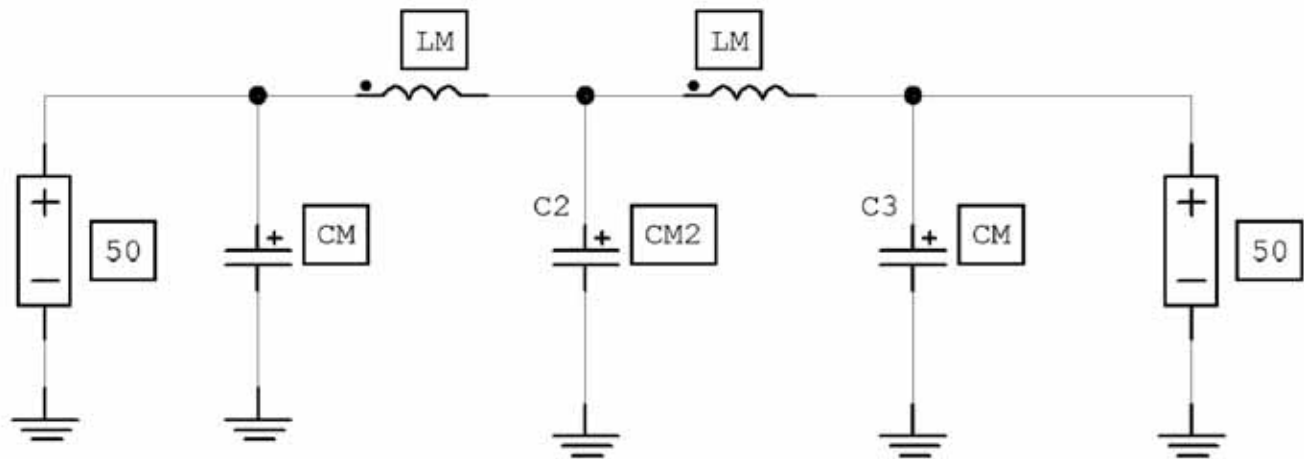
Figure 12. Fifth-Order PI-Topology Low-Pass Filter

Figure 12 shows the general architecture of a fifth-order, low-pass filter using the PI-topology. After design of a 0.17 dB ripple Chebyshev filter with a peak frequency of 868 MHz (F_{ERCUT} = 908.6 MHz), the following component values are obtained between 50 Ω termination impedances:

- CM = 4.561 pF
- LM = 11.79 nH
- CM2 = 7.458 pF

It is generally sufficient to use the nearest available standard 5% component tolerance values. Making these substitutions results in the following set of component values:

- CM = 4.7 pF
- LM = 12 nH
- CM2 = 7.5 pF

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4.3.6.5. Simulation of Actual Filter Frequency Response

An ideal frequency response is not possible in practice because it is necessary to use inductors and capacitors with not only finite Qs but also with internal self-resonances due to parasitic elements. These factors, as well as parasitic effects due to board layout, may cause the actual frequency response to be degraded relative to the ideal response shown in Figure 11.

The effects of using non-ideal components can be predicted by simulation with SPICE models obtained from the manufacturers of discrete components (e.g., Murata, CoilCraft, etc.). Figure 13 shows the simulated frequency response of this low-pass filter design implemented with the real (lossy) 5% components given above. Although the filter attenuation at the second harmonic frequency (1732 MHz) is very strong (58.8 dB) and far exceeds our design goal of 28 dB minimum, the attenuation at 868 MHz is also very high: ~2.59 dB. The introduced losses and parasitics deteriorated the filter response significantly and increased the useful band attenuation to an unacceptable level.

S21[dB] Non-Ideal 5th order Chebyshev response with 20% passband reflection and 908.6M cuttoff
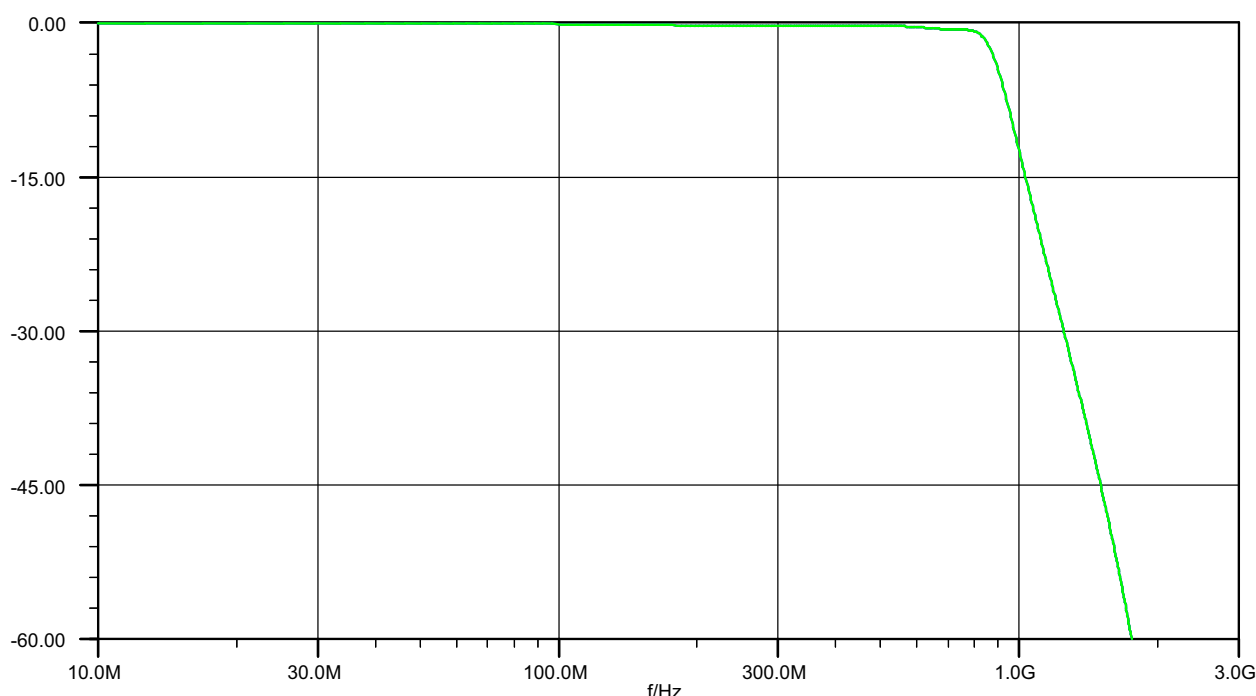
Figure 13. Non-Ideal Simulated Freq Response of 0.17 dB Chebyshev Filter (Fo = 868 MHz) with 5% Elements

A possible solution is to adjust the filter first in the simulator and after that on the bench. Basically, some harmonic attenuation can be sacrificed to get lower attenuation at 868 MHz. The new set of element values after tweaking are:

- CM = 2.7 pF
- LM = 9.1 nH
- CM2 = 5.1 pF

The non-ideal filter response after adjustment is given in Figure 14. Here, the cutoff frequency is shifted up, and, thus, the simulated attenuation at 868 MHz is approximately 0.32 dB. The second harmonic (1732 MHz) attenuation is still ~29 dB, 1 dB better than the targeted 28 dB. Also, due to the parasitic, the attenuation decreases at very high frequencies (10th harmonic and above), but is still around –40 dB, which is far enough for those low-level high harmonics. The filter attenuation at the higher harmonics easily exceeds our design target of 28 dB, thus validating the choice of filter type, order, and passband amplitude ripple.

S21[dB] Non- Ideal 5th order Chebyshev response with 20% passband reflection after tweaking
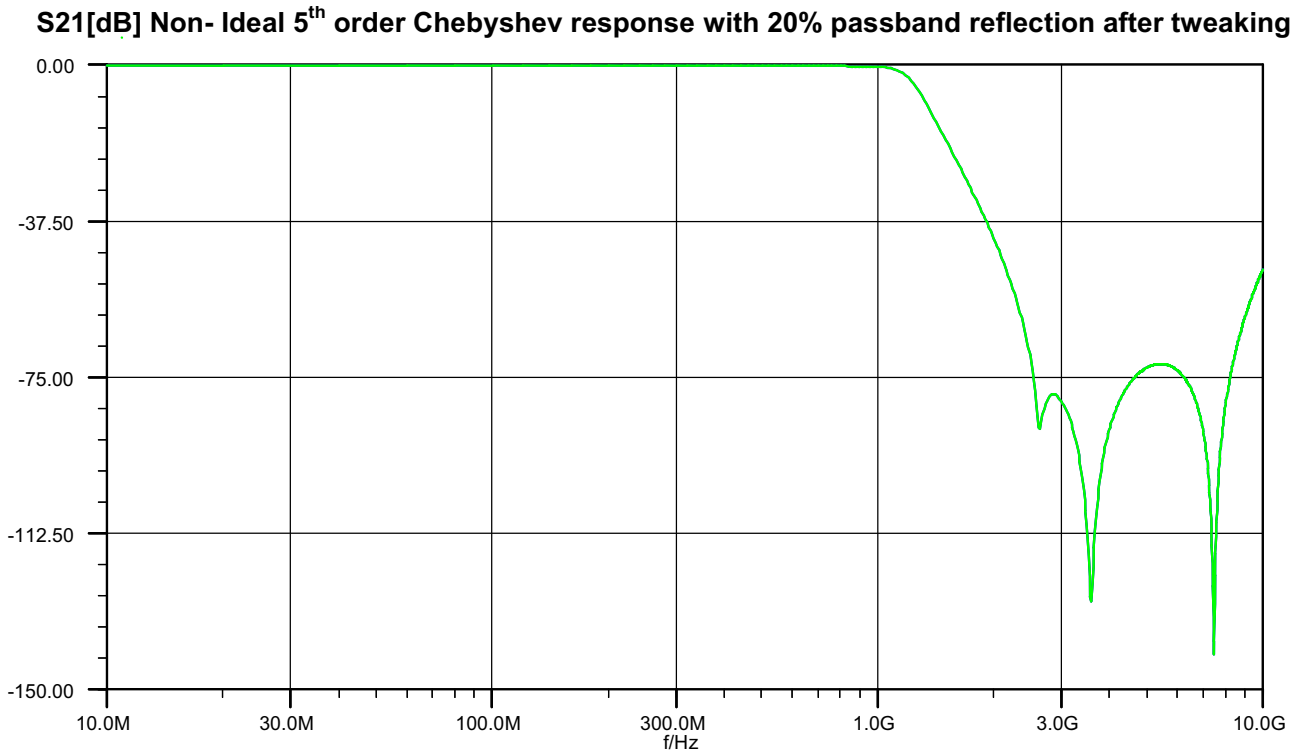
**Figure 14. Non-Ideal Simulated Freq Response of 0.17 dB Chebyshev Filter
after Tweaking (Fo = 868 MHz)**

However, it should be clearly understood that Silicon Labs does not guarantee that a fifth-order, low-pass filter design is appropriate for all customer applications. Depending upon the applicable regulatory standard and desired output power level, the filter order may need to be modified to suit a particular customer's needs.

It is apparent that there are now transmission zeros in the simulated frequency response. These transmission zeros (e.g., near 3.6 GHz and 7.45 GHz in Figure 14) are due to self-resonances in the discrete components. The shunt capacitors in the filter network (i.e. CM and CM2) exhibit a series self-resonance at some frequency, while the series inductors (i.e. L0, LM, and LM2) exhibit a parallel self-resonance at some frequency. The presence of such transmission zeros may help to "bend down" the attenuation curve more quickly, resulting in improved attenuation at lower harmonic frequencies, but at the cost of degraded attenuation at higher harmonic frequencies. It is not advisable to rely too heavily upon "tuning" of these transmission zeroes to aid in meeting harmonic performance.

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4.3.6.6. Combining the LPF with the Output Match

The methodology used for the design of the low-pass filter was for a filter with a 1:1 impedance transformation ratio. That is, if the antenna impedance was $R_{ANT} = 50\ \Omega$, then the impedance seen looking into the input of the low-pass filter at CM is also 50 Ω (at the fundamental frequency). Thus, our calculations for impedance matching components L_X and C_X remain unchanged. The resulting schematic for the output match and low-pass filter is shown in Figure 15.
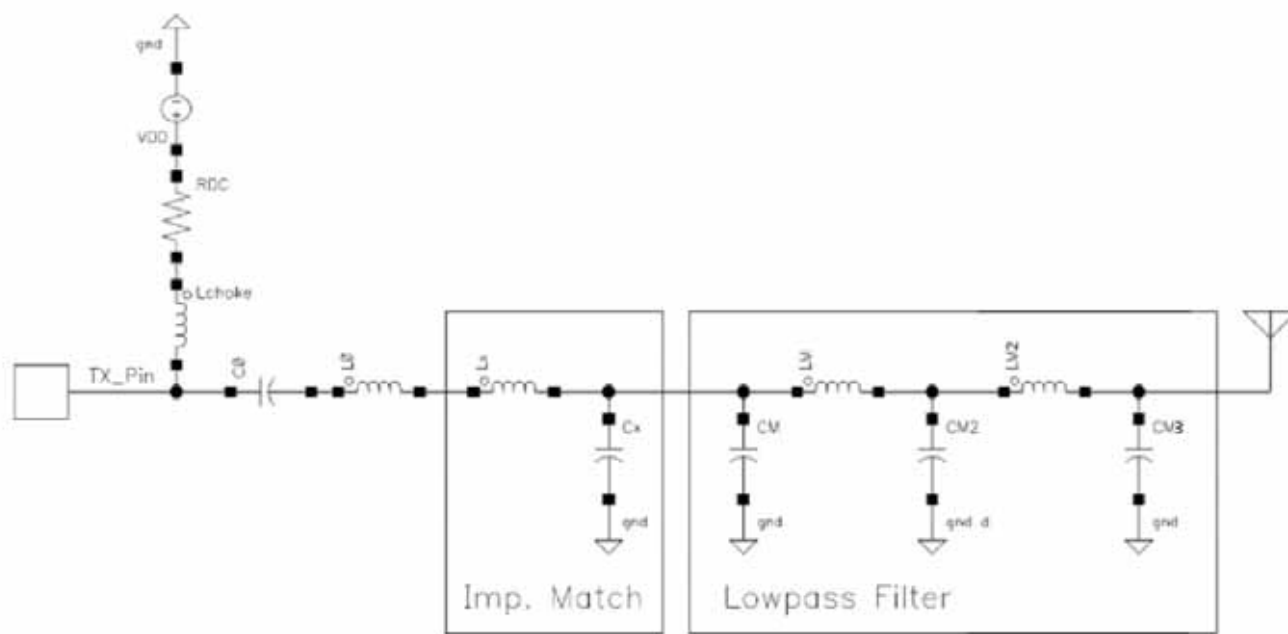
Figure 15. Schematic of Output Match and Low-Pass Filter

However, it is quickly apparent that this schematic may be simplified. As discussed previously, series inductors L_0 and L_X may be combined into one equivalent series inductance. Shunt capacitors C_X and C_M may be combined in a similar fashion. After simplification, the schematic appears as shown in Figure 16. The combined value of values $L_0 + L_X = 19$ nH, while the combined value of $C_M + C_X = 6$ pF.
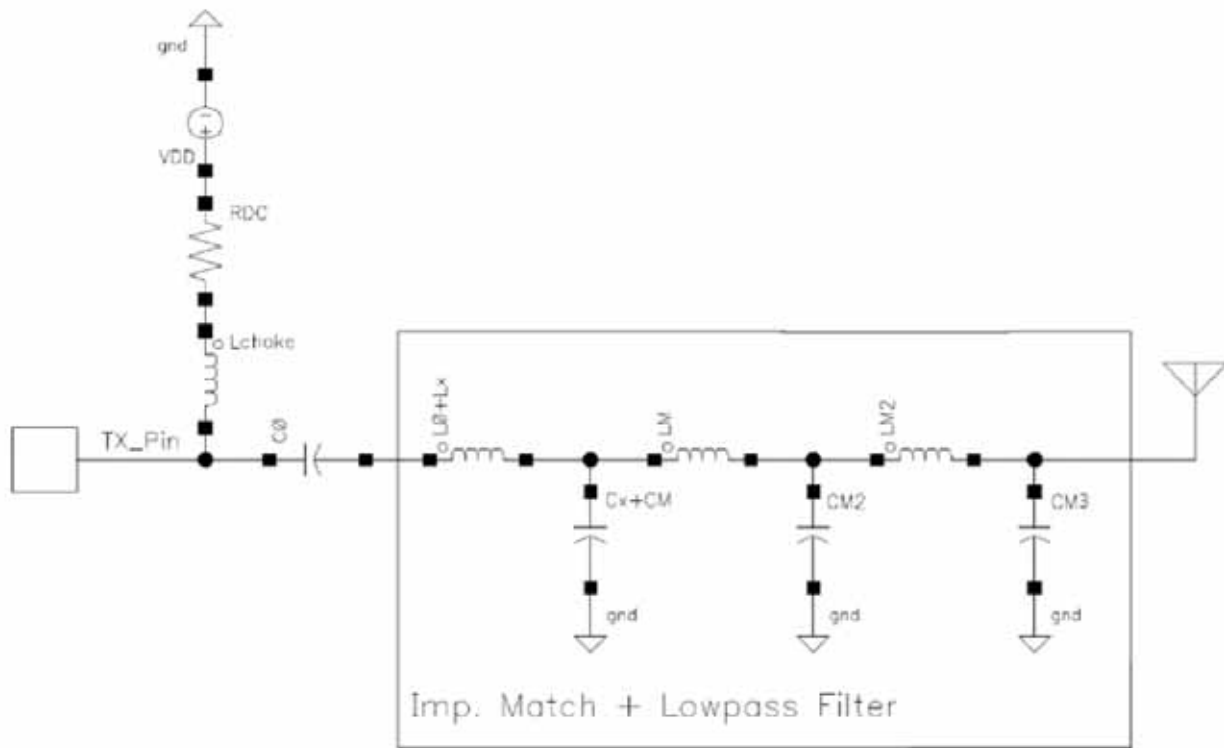
Figure 16. Schematic of Output Match and Low-Pass Filter (Simplified)

After the filtered class E Tx match is finalized, some bench tuning is also worth trying. As mentioned earlier, during the adjustment process, it was seen that the efficiency can be improved slightly if the CM capacitor is reduced to 2.7 pF. Again, this sacrifices some second-harmonic attenuation, but still the harmonic spectrum complies with large margin (see Figure 17).

The final class E Split TX match component values are given in Table 3 in "2.1.1. Si4455 CLE Split TX/RX Board Configuration: Component Values and Performance" on page 3.

4.3.6.7. Final Measurement of Harmonic Spectrum of the 13 dBm Class E Match

The conducted output power spectrum of the final circuit is shown in Figure 17. These results are measured at the TX output power level setting of 31h of the Si4455 RFIC with 22.8 mA total current consumption at 3.2 V supply voltage. As can be seen, the output power is approximately 0.5 dB lower than that without a filter, i.e., the real lossy filter attenuation is approximately 0.5 dB, but, due to the reduced CM, the efficiency improved, and the total IC current is only 22.8 mA.
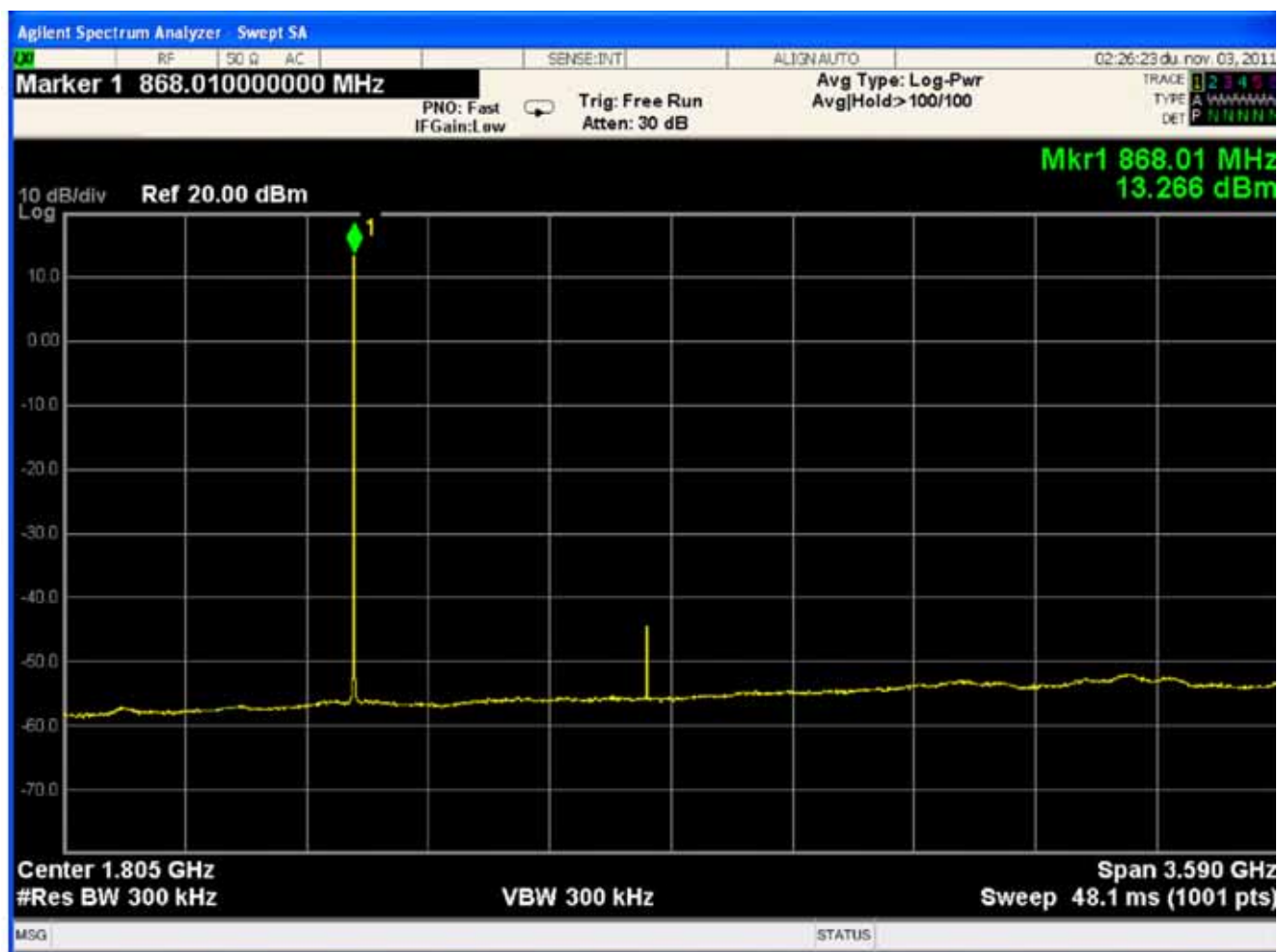
Figure 17. Filtered Harmonic Spectrum at Power State 31h (with 22.8 mA total IC Current) of the 13 dBm Si4455 Class E Match (Fo = 868 MHz, also Given in Table 3)

4.3.6.8. Final Measurement of Harmonic Spectrum of the 10 dBm Class E Match

In theory, the 10 dBm Class E design should be the same as the 13 dBm. Only the power level is reduced properly by a lower power level setting. However, during bench adjustment, it turned out that the efficiency at low power levels can be improved further if the C0 value is increased. The conducted output power spectrum of the final 10 dBm circuit (given in Table 1) is shown in Figure 18. These results are measured at the TX output power level setting of 19h of the Si4455 RFIC with 16.4 mA total current consumption at 3.2 V supply voltage.
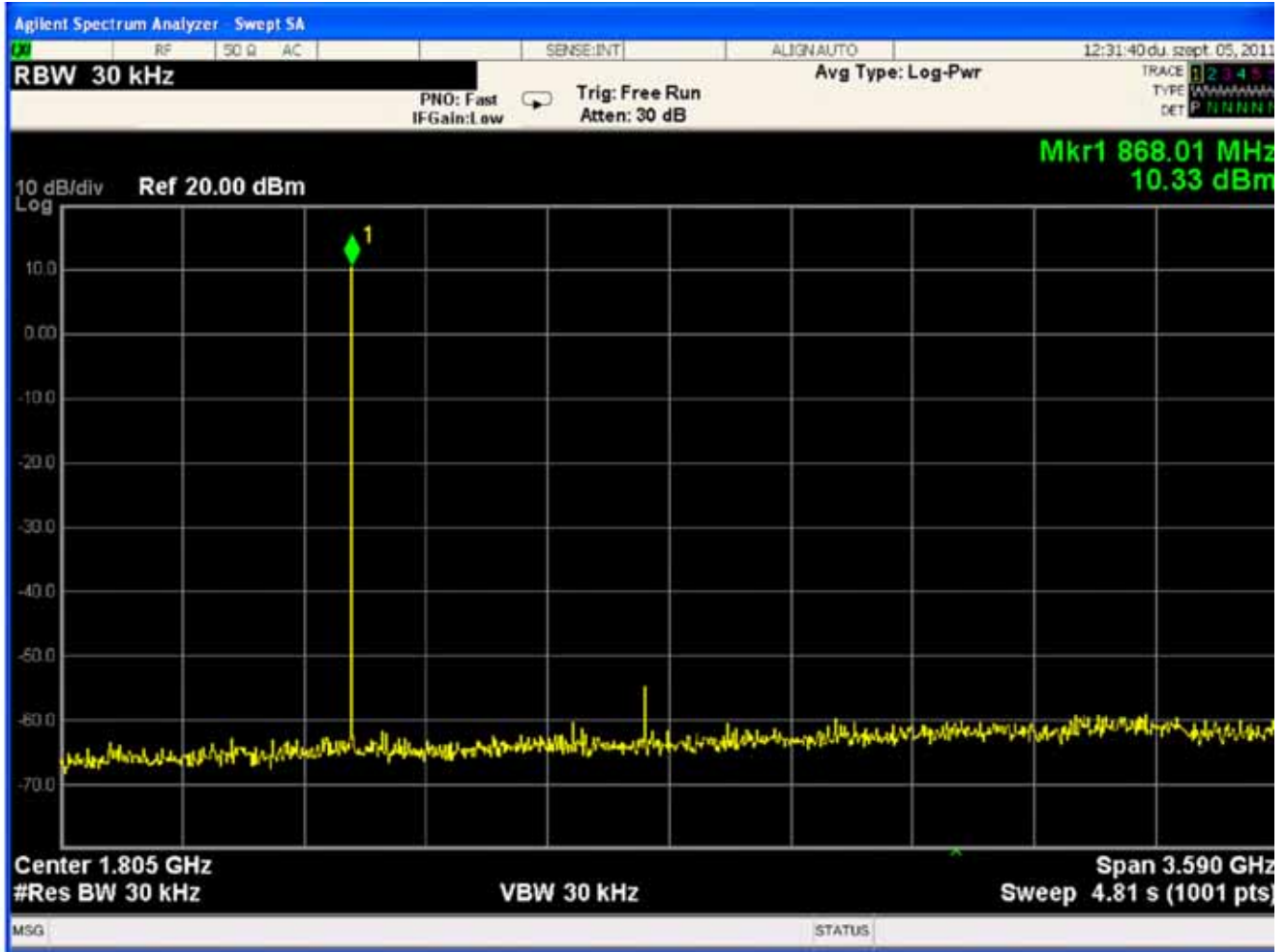
Figure 18. Filtered Harmonic Spectrum at Power State 19h of the Tuned 10 dBm Si4455 Class E Match (Fo = 868 MHz; See Table 3 for Component Values)

4.3.7. Summary of Match

This completes the steps of the match design process for the Split TX/RX board configuration. This match design process may be used to obtain matching component values at any desired operating frequency. A summary table of these matching component values is shown in Tables 1 and Table 2.

4.4. Detailed Matching Procedure for Direct Tie Board Configuration

In the Direct Tie board configuration, the TX and RX paths are tied directly together without the use of an RF switch, as shown in Figures 5 and 7. Careful design procedures must be followed to ensure that the RX input circuitry does not load down the TX output path while in TX mode, and that the TX output circuitry does not degrade receive performance while in RX mode.

The RX input circuitry of the EZRadio 2 family of chips contains a set of switches that aids in isolation of the TX and RX functions. These switches are implemented internally as shown in Figure 19.
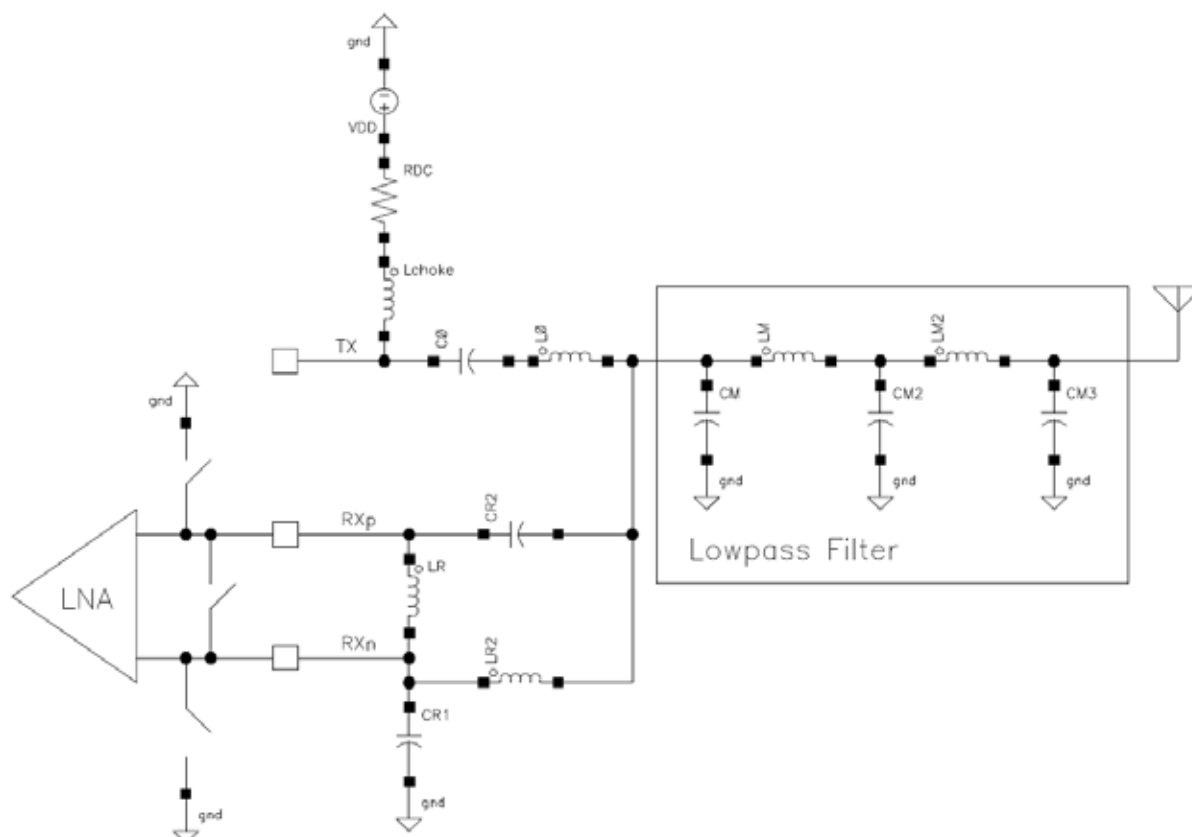
Figure 19. RX Input Switches for Direct Tie Operation

The three switches are activated simultaneously upon entering TX mode. They are opened only in RX mode and closed during all other modes (including TX mode).

Closing these switches during TX mode effectively shorts the RXp and RXn input pins together and also shorts them to GND. The effective circuit may be redrawn as shown in Figure 20. Note that inductor LR2 and capacitor CR2 have been placed in parallel by the closure of the switches and are connected to GND. If the values of these components are chosen for resonance at the desired operating frequency, a very high impedance is presented to the TX path resulting in very little degradation in TX output power. Also, by shorting the input pins of the LNA together and simultaneously to GND, the LNA is protected from the large signal swing of the TX signal. This feature allows connection of the TX path to the RX path without damage to the LNA.
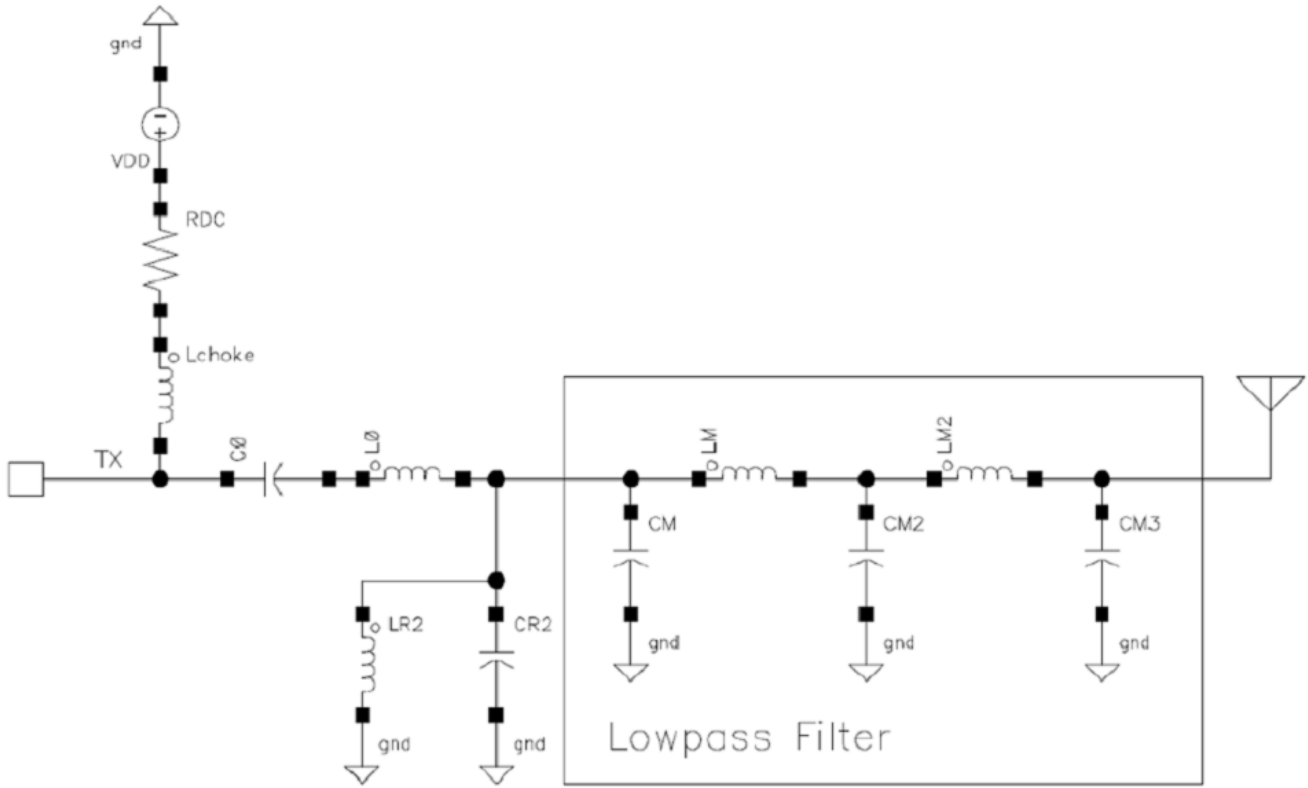
Figure 20. Effective Direct Tie Circuit in TX Mode

In RX mode, the output transistors of the PA are in the OFF state, and the impedance seen looking back into the TX pin is comprised mostly of the output capacitance of the transistors. (The impedance of the pull-up inductor L_{CHOKE} is quite high and may be ignored for this discussion.) This OFF stated PA output capacitance value (C_{PAOFF}) is not much different from the ON STATED one; typically, it is 10 to 15% higher (i.e., a good estimate is ~1.4 to 1.5 pF for the Si4455). For a Class E match, this PA capacitance is effectively in series with matching capacitor C0 and will result in series-resonance with inductor L0 at some frequency, as shown in Figure 21. At this series-resonant frequency, the input to the LNA matching network (LR2-CR2-LR1-CR1) is effectively shorted to GND and thus significantly degrades receive performance. Since the PA output capacitance C_{PAOFF} is fixed, it is necessary to choose L0 and C0 to ensure that this series-resonance does not excessively degrade RX performance at the desired operating frequency. It may be necessary to alter the values of L0 (variation of C0 is less efficient because it is in series with the fixed C_{PAOFF}) slightly away from their calculated optimum values in order to accomplish this goal, thus slightly degrading TX performance in an effort to minimize the impact to RX performance.

With the typical C_{PAOFF} values of Si4455 RFIC family, this effect is most critical on the upper frequency bands (868/915M). On lower frequency bands (315 to 434 M) it usually does not cause any problems, and the DT TX match element values are identical to the values of the Split TX/RX configuration.
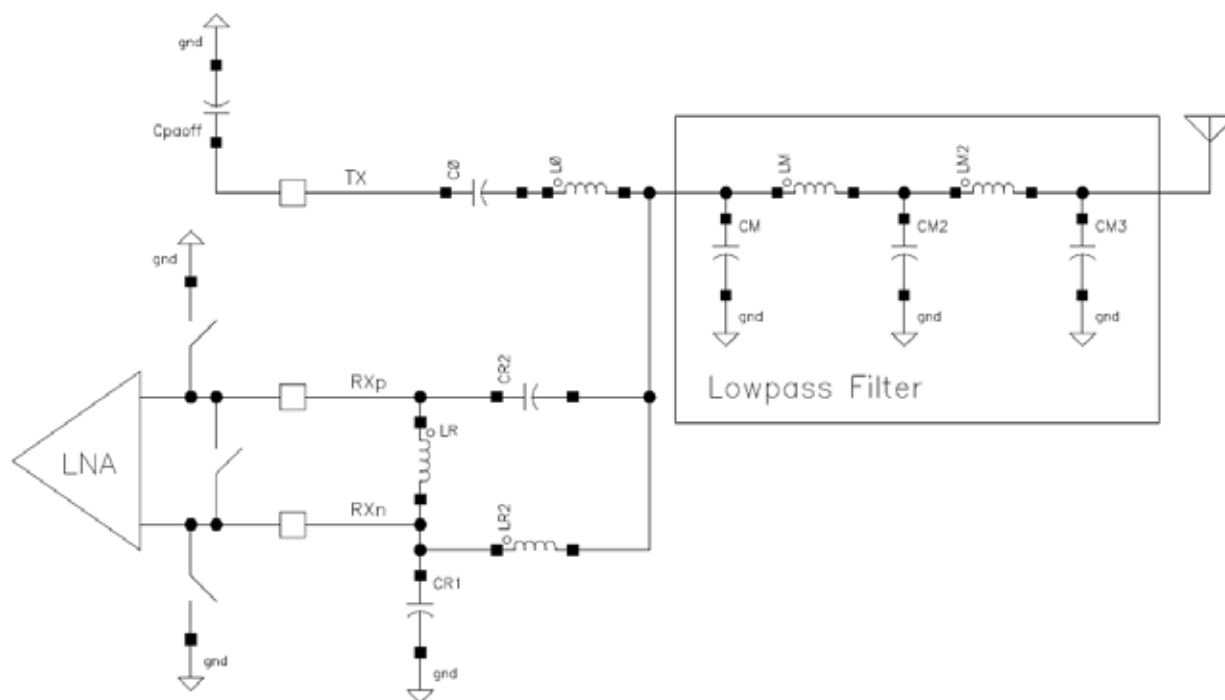
Figure 21. Effective Direct Tie Circuit in RX Mode

We next provide further detail about each step of the matching procedure for the Single Antenna with Direct Tie board configuration. We again assume a general chip supply voltage of V_{DD_RF} = 3.3 V. Our design example will be constructed for the Si4455 for the 868 MHz ETSI band with a targeted output power level of +13 dBm.

4.4.1. Steps #1–6: Same Design Procedure as for Split TX/RX Board Configuration

Steps 1 through 6 are exactly the same as those shown in "4.3. Detailed Matching Procedure for Split TX/RX Board Configuration" on page 18.

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4.4.2. Step #7: Design RX Input Match

In Step #7, we designed an impedance matching network for the differential RX input. The RX matching network is composed of a total of four inductors and capacitors (LR2-CR2-LR1-CR1). The goals for this network are as follows:

- Match the LNA input to a 50 Ω source impedance (i.e., the antenna)
- Provide a single-ended to differential conversion function (i.e., a balun)
- Ensure that LR2-CR2 are parallel-resonant at the desired operating frequency

The design equations (and their mathematical derivations) for selection of the matching component values are discussed in detail in "AN643: Si446x/Si4362 RX LNA Matching". The following equations are introduced here without proof or further discussion; refer to AN643 for more details.

$$L_{R2} = \frac{\sqrt{50\Omega \times R_{LNA}}}{\omega_{RF}}$$

Equation 11.

$$C_{R2} = \frac{1}{\omega_{RF}^2 \times L_{R2}}$$

Equation 12.

$$C_{R1} = 2 \times C_{R2}$$

Equation 13.

$$L_{LNA} = \frac{1}{\omega_{RF}^2 \times C_{LNA}}$$

Equation 14.

$$L_M = 2 \times L_{R2}$$

Equation 15.

$$L_{R1} = \frac{L_{LNA} \times L_M}{L_{LNA} + L_M}$$

Equation 16.

Note that our goal of parallel-resonance between LR2 and CR2 is inherently satisfied, as evidenced by Equation 12.

At any given frequency, the differential input impedance at the RX pins of the chip may be represented by an equivalent parallel R-C circuit; their values are represented by the parameters R_{LNA} and C_{LNA} in the above equations. It is necessary to know these equivalent circuit values at the desired frequency of operation, prior to constructing the match.

The differential input impedance of the RX port on the Si446x RFIC (which can be applied to the Si4x55 RFIC as well) is provided in "AN643: Si446x/Si4362 RX LNA Matching". The values of R_{LNA} and C_{LNA} at a desired operating frequency of 868 MHz are found to be R_{LNA} = 380 Ω and C_{LNA} = 1.09 pF. After plugging these values into the above equations, the following ideal matching component values are calculated:

- LR2 = 25.27 nH
- CR2 = 1.33 pF
- LR1 = 19.15 nH
- CR1 = 2.66 pF

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In practice, it is often necessary to slightly modify the matching component values suggested by the above equations. Any printed circuit board layout has parasitics, such as trace inductance or component pad capacitance, and these may have an effect upon the circuit. Silicon Labs has empirically determined that, if 0402-size wire-wound or multilayer inductors are used on the Direct Tie reference board designs available on our web site, the actual component values are as shown in the 868 MHz rows in Table 3 for the wire-wound case, and reproduced below:

- LR2 = 24 nH
- CR2 = 1 pF
- LR1 = 20 nH
- CR1 = 3 pF

The above inductor element values are not available in multilayer type; so, new bench optimized multilayer RX match elements are necessary and are given in Table 4 on page 6.

Although not required, it is useful to measure the input impedance seen looking into the RX match in both RX mode as well as TX mode. Obviously, it is desireable to verify a good match to 50 Ω while in RX mode in order to obtain optimum sensitivity. However, it is also useful to verify that the network provides a high impedance while in TX mode (when the switches at the input of the LNA (see Figure 21) are in their CLOSED position, and thus LR2 and CR2 form a high-impedance, parallel-resonant network, which isolates the RX path from the TX path); otherwise, the RX circuitry may excessively load down the TX path. Specifically, it may be necessary to slightly adjust the values of LR2 and/or CR2 to achieve optimum parallel resonance at the desired frequency of operation.

The isolation in TX mode is more critical with multilayer inductors because this type has lower Q (higher loss), and the values are available in rarer steps; so, it is more difficult to both achieve high impedance at LR2-CR2 parallel resonance and to tune the resonance exactly to the operating frequency.

The actual measured impedance of the 868M multilayer RX match while in TX mode is shown in Figure 22 and confirms the expectations of sufficient isolation. The measured impedance at 868 MHz is ~452 Ω + j593 Ω, which corresponds to a parallel R-C equivalent of 1.2 kΩ –0.196 pF. This slight parallel capacitance (~196 fF) may be ignored.
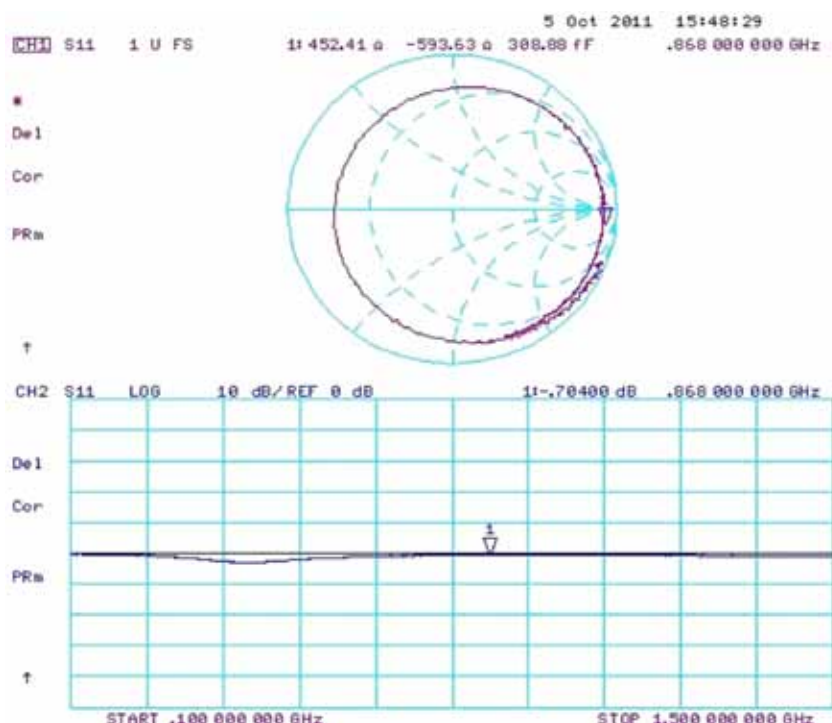
Figure 22. RX Match Input Impedance in TX Mode (Multilayer 868M Type)

The measured impedance at the input of the multilayer RX matching network while in RX mode is shown in Figure 23. It is observed that the input impedance is quite close to 50 Ω, with the network providing S11 with better than 15 dB return loss.
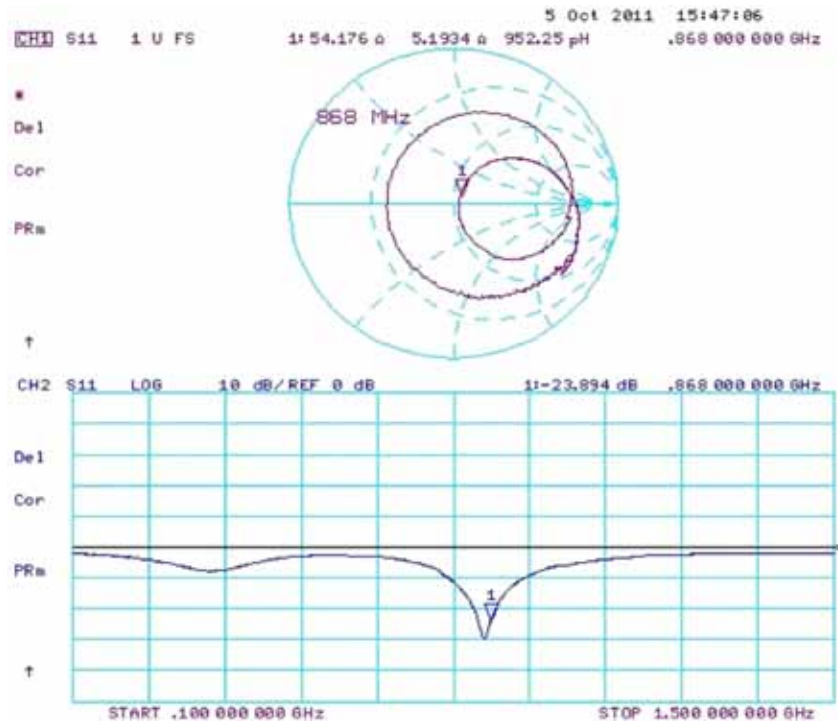
Figure 23. RX Match Input Impedance in RX Mode. Multilayer 868M type

4.4.3. Step #8: Slightly Modify the Value of L0

In Step #8, we deliberately mis-tune the value of matching inductor L0 slightly away from its optimum value, as determined in Steps #1-6. As illustrated in Figure 21, the series-resonance of L0-C0-CPAOFF has the potential for significantly degrading the RX performance by placing a (near) short to GND at the input of the RX matching network. It is important that this series-resonant frequency be adjusted to fall sufficiently far away from the desired operating frequency in order to minimize its effect upon RX sensitivity.

This is accomplished by deliberately increasing or decreasing the value of L0. Here, the variation of C0 is not efficient since it is in series with the fixed CPAOFF and thus has higher deviation from its optimum class-E value than would be necessary to achieve the same detuning.

For the Si4455, the decrease of L0 is usually required at 868/915 MHz to push the series resonance. This pushes the unwanted resonance lower or higher in frequency and minimizes its effect upon RX performance. A typical aim is to suffer less than 2 dB sensitivity degradation in direct tie mode compared to the split TX/RX case.

Some post-tuning of capacitor CM may also be required to improve Class-E operation in TX mode after the change in value of L0.

The value of PA output capacitance in its OFF state may be somewhat different than the value of shunt drain capacitance C_{SHUNT} (discussed in "4.3.3. Step #3: Calculate the Required Value for ZLOAD" on page 19). The value of C_{PAOFF} may be measured with a network analyzer connected to the TX output pin with all matching components removed, except for those providing dc bias (i.e., L_{CHOKE} and R_{DC}). Silicon Labs has performed this measurement and determined the value of C_{PAOFF} to be ~ 1.5 pF in the frequency range of 868 MHz to 950 MHz and 1.4 pF on low bands (315/434M). This is shown by the impedance measurement of Figure 24. The value of L_{CHOKE} must be chosen appropriately to provide a very high impedance at the frequency of interest; otherwise, the measured value of C_{PAOFF} may be affected.
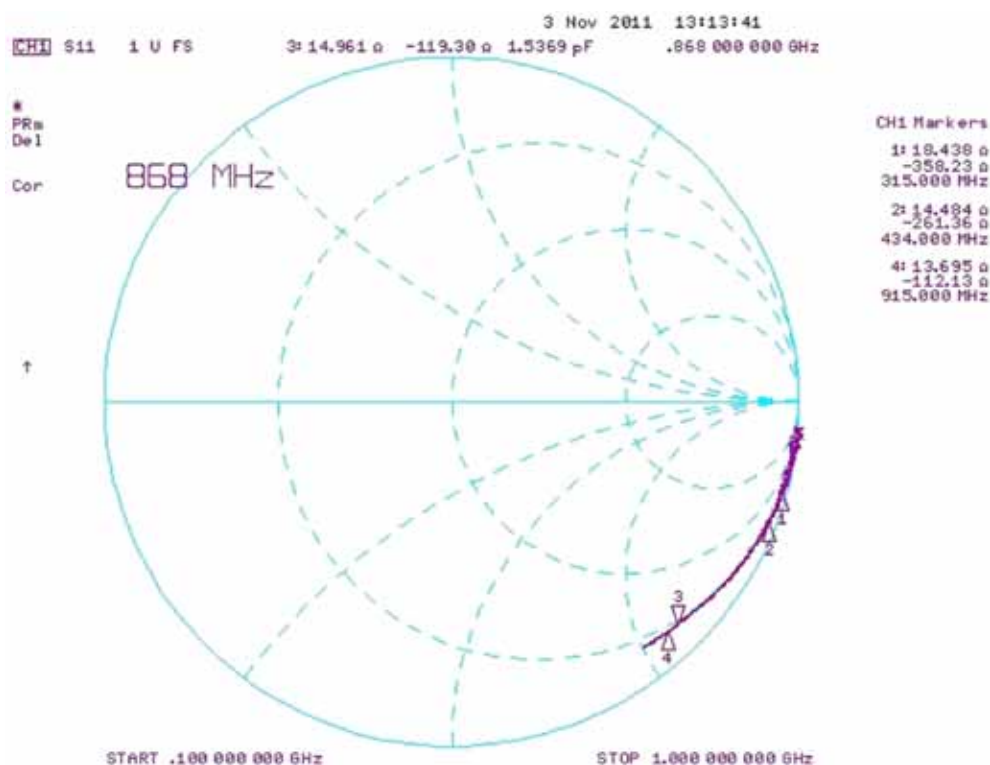
Figure 24. PA Output Capacitance Measurement of Si4455 in OFF State

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Once the value of C_{PAOFF} has been determined, its effect upon RX performance may be estimated. Continuing with our design example at 868 MHz with the 13 dBm wire-wound split TX/RX board design, we find initial values of L0–C0 to be:

- L0 = 19 nH
- C0 = 3.6 pF

This value of capacitance of C0 is in series with C_{PAOFF} = 1.5 pF, resulting in an equivalent series capacitance of C_{EQUIV} = 1.06 pF. The series-resonant behavior of the resulting L-C circuit may be simulated and is shown in Figure 25 (here the S21 of the TX path is simulated from the filter outputs to the DT point with the L0-C0-CPAOFF part). It can be observed that this L0-C0-CPAOFF circuit introduces only ~0.8 dB of loss at 868 MHz, which is mostly due to the filter attenuation. Since this circuit is directly connected to the input of the RX match, this results in approximately 0.8 dB of degradation in RX sensitivity, which is acceptable.
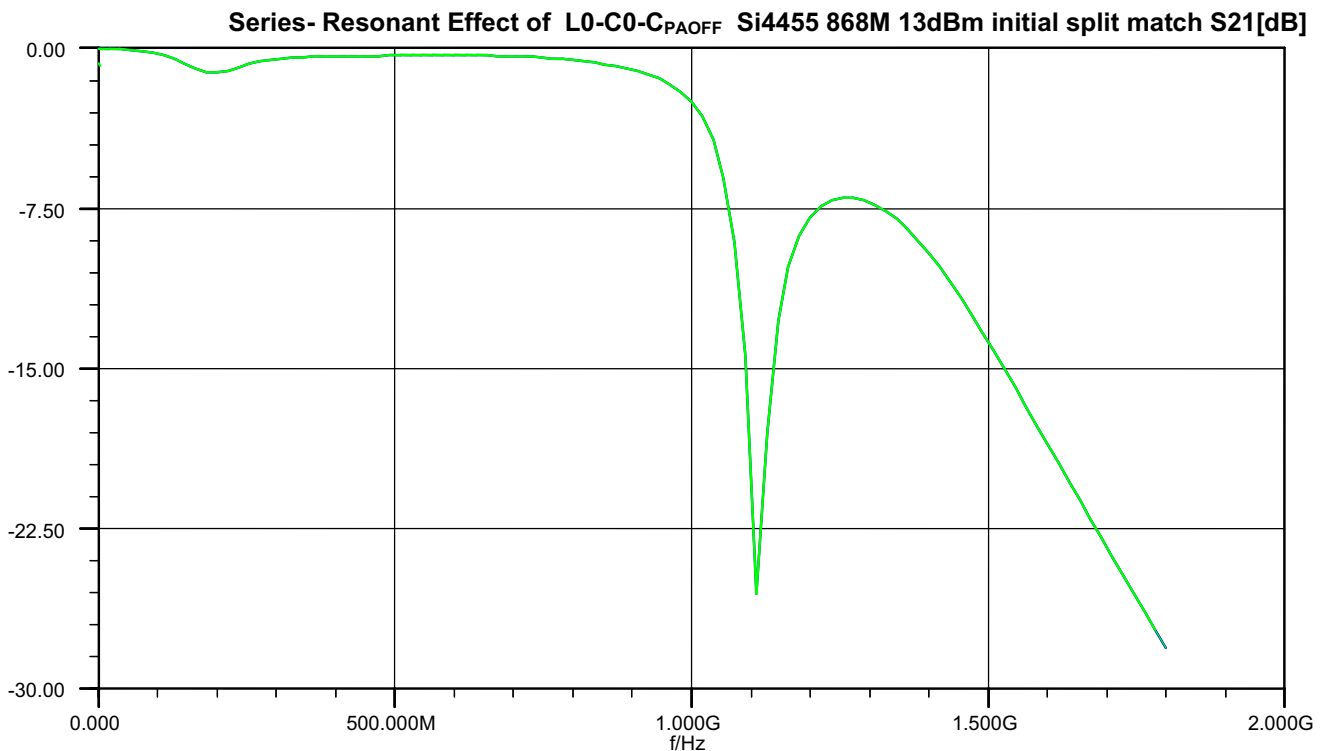
Figure 25. Series-Resonance Behavior of Initial L0-C0 Circuit of Si4455 13dBm Split Class E Match

Unfortunately, the situation is more critical for the Si4455 10 dBm direct tie. There, the initial split C0 value is much higher (see Table 1 on page 3) in order to achieve better efficiency at reduced power levels with the initial values of:

- L0 = 19 nH
- C0 = 15 pF

The parasitic L0-C0-CPAOFF series resonance curve is shown in Figure 26. As can be observed, due to the higher C0, the resultant equivalent capacitance is 1.36 pF, and, thus, the resonance is at lower frequencies closer to the useful band. It results in attenuation of ~2.5 dB according to the simulations. In real bench circumstances, the degradation in RX mode was even higher, approximately 3.5 dB, which is not acceptable.

The resonant frequency of these circuit components may be shifted further upwards (away from the desired operating frequency) by decreasing the value of L0. Using our rule-of-thumb of decreasing L0 by ~20%, we arrive at a modified value of L0 = 15 nH. In theory, with the 20% L0 variation, the Class E operation in TX mode is still satisfactory, and, usually, the sensitivity degradation in RX mode improves to be less than ~2 dB.

However, for the +10 dBm 868 MHz Si4455 DT match, the bench test (even of this modified circuit) still did not show adequate sensitivity improvement in RX mode.

Therefore, the L0 was decreased further to 12 nH with a parallel increase of C0 to keep the optimum Class E TX operation. Here, it important to note that the increase of the C0 capacitor will have a negligible effect on the parasitic series resonant frequency since the value of C_{PAOFF} is much lower than that of C0, and, thus, C0 determines the resonance. Simulation of the series-resonant behavior of the modified circuit is shown in Figure 27.

It can be seen that the loss at 868 MHz has now been improved significantly to only ~0.9 dB in the simulations. In the bench test, the suffered RX sensitivity degradation is only ~1.1 dB, which is very close to the simulated value. While this still represents a 1.2 dB reduction in RX sensitivity, this is a good compromise between TX and RX performance.
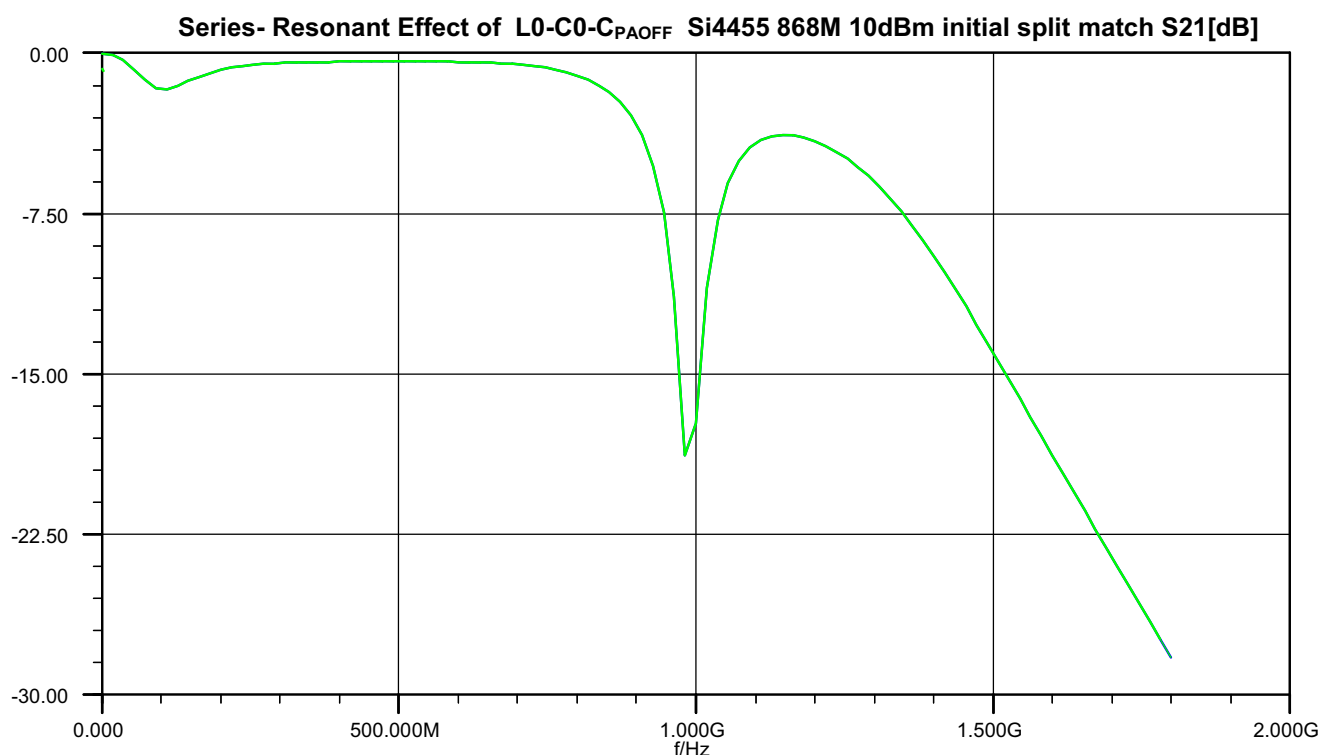
Figure 26. Series-Resonance Behavior of Initial L0-C0 Circuit of Si4455 10 dBm Split Class E Match

Series- Resonant Effect of L0-C0-C$_{PAOFF}$ Si4455 868M 10dBm of Modified DT match S21[dB]

magdb(S(2,1))   magdb(S(1,2))
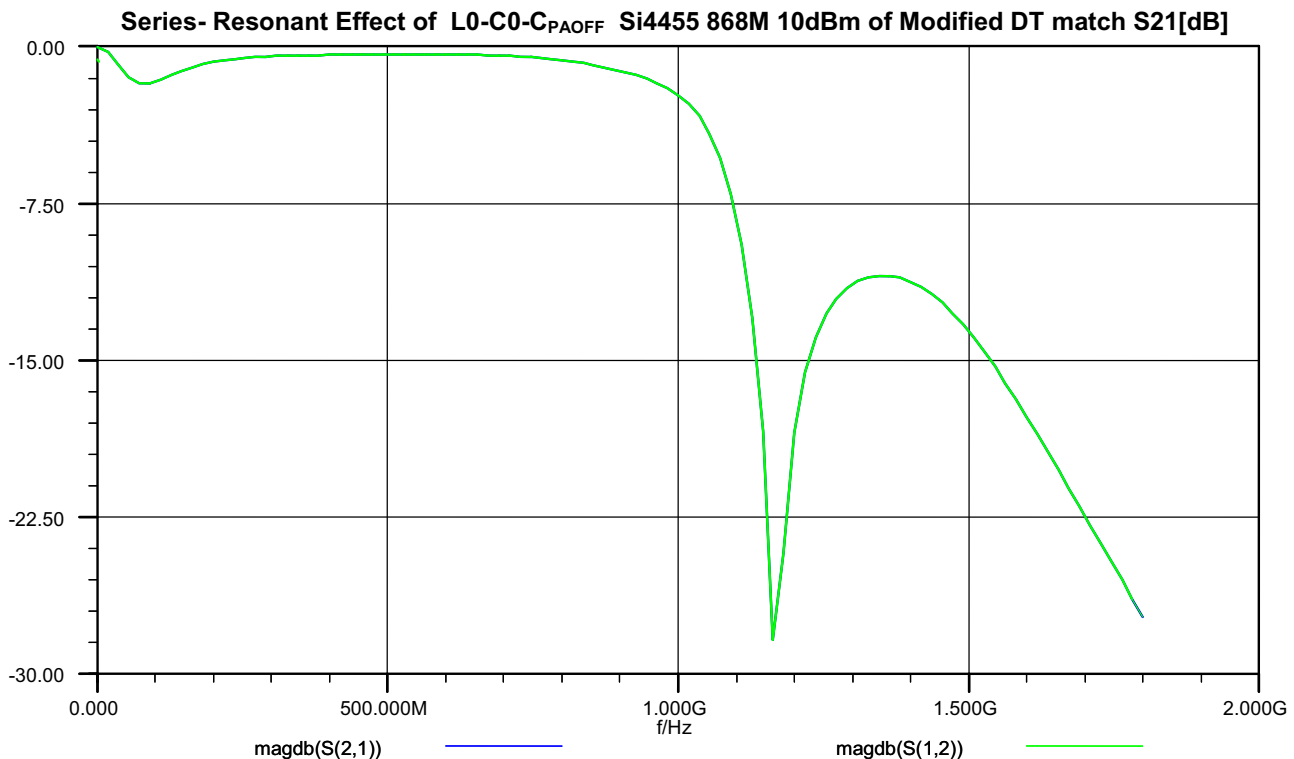
Figure 27. Series-Resonance Behavior of Modified L0-C0 Circuit of Si4455 10 dBm DT Class E Match

It would also be possible to increase the resonant frequency of the L0-C0-C$_{PAOFF}$ circuit by decreasing the value of C0 instead of L0. However, since C0 is in series with C$_{PAOFF}$, and, moreover, the C0 value is significantly higher, a much larger change in value must occur to provide the same amount of mistuning. This stronger mistuning will result in an even greater reduction in performance in TX mode. Therefore, tuning of L0 is preferred and generally results in a better compromise between TX and RX performance.

This increase in the value of L0 is usually required only when working in the upper frequency bands (e.g., 868/915/950 MHz). In the lower frequency bands (315/390/434 MHz), the values of L0 and C0 obtained for the Split TX/RX board configuration usually continue to work well with the Direct Tie board configuration.

In the final circuit realization on Silicon Labs reference design boards, the value of capacitor CM was reduced to 1.5 pF to provide slightly better TX output power. The final Si4455 element values with wire-wound inductors are summarized in Table 3 on page 5. For Multilayer inductors, the same values are given in Table 4 on page 6.

Note that some minor degradation in both TX and RX performance is expected for a Direct Tie configuration. That is, it is not possible to directly connect the TX and RX paths together and achieve perfect isolation between the two circuit functions; each path will result in some amount of unwanted loading to the other path, and, thus, there is some small degradation in performance (relative to a Split TX/RX board configuration in which the TX and RX paths remain entirely separate). The choice of matching inductor L0 heavily impacts the trade-off between optimizing for TX output power at the expense of degraded RX sensitivity, or vice versa. A value may generally be found that achieves a good compromise between the two, typically resulting in less than 1 dB reduction in TX output power and no more than 2–3 dB reduction in RX sensitivity. Some adjustment of the final values of L0 and CM may be necessary to achieve this best compromise.

4.4.4. Summary of Match

This completes the steps of the match design process for the Direct Tie board configuration. This match design process may be used to obtain matching component values at any desired operating frequency.

APPENDIX—MEASURED SPECTRUM PLOTS

The following figures present some measured spectral data plots on different CLE board configurations at a variety of frequencies given in "2. Summary of Matching Network Component Values" on page 2. Measured results for circuit realizations with both wire-wound inductors and multi-layer inductors are presented.

Si4455 Measured Plots

### Si4455 Split TX/RX Board CLE Configurations with Wire-Wound Inductors
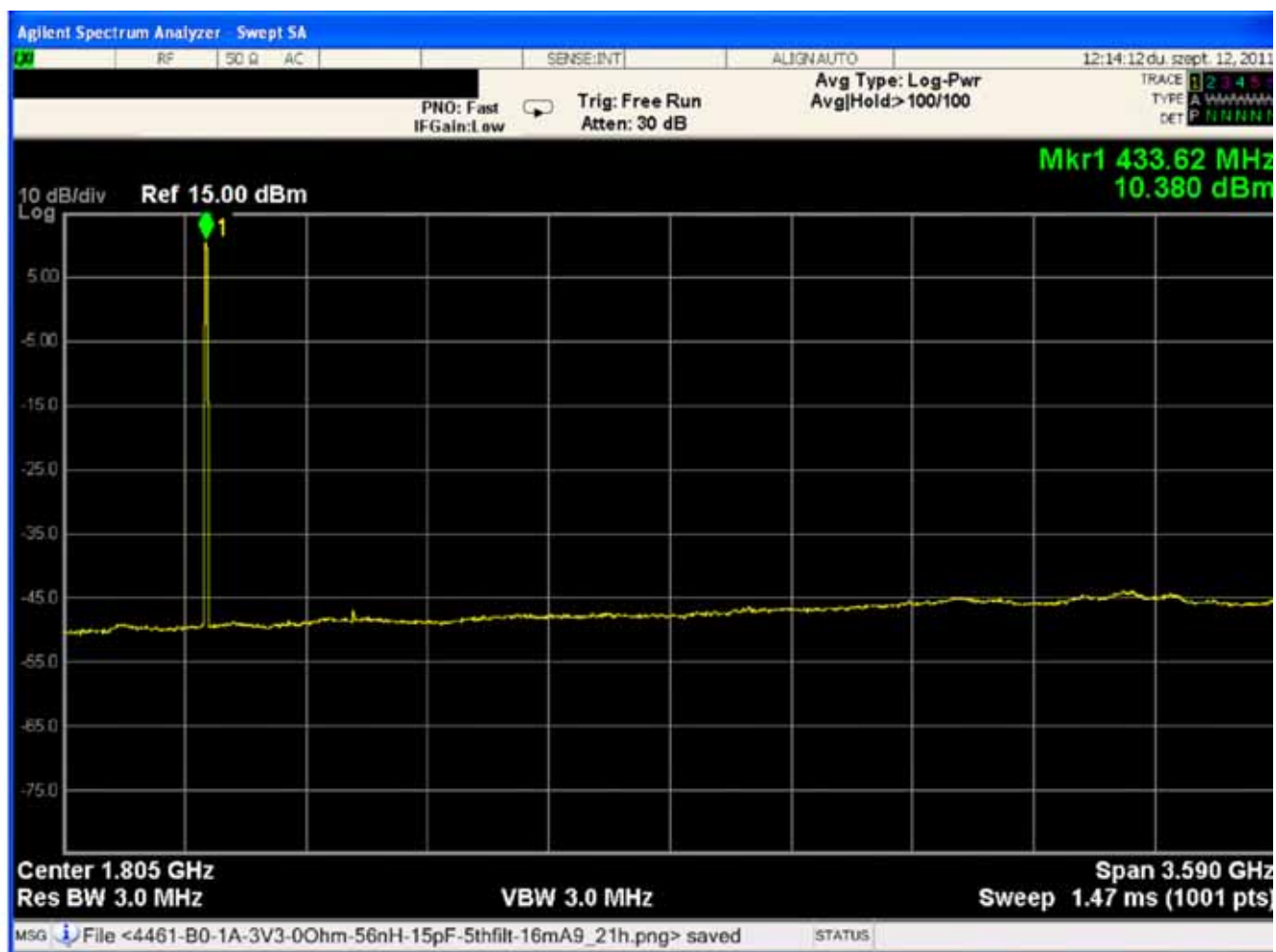
Figure 28. Si4455 10 dBm Split TX/RX Board at 434 MHz with Wire-Wound Inductors, V$_{DD}$ = 3.2 V, DDAC[6:0] field in the PA_PWR_LVL register is 19h, 16.9 mA
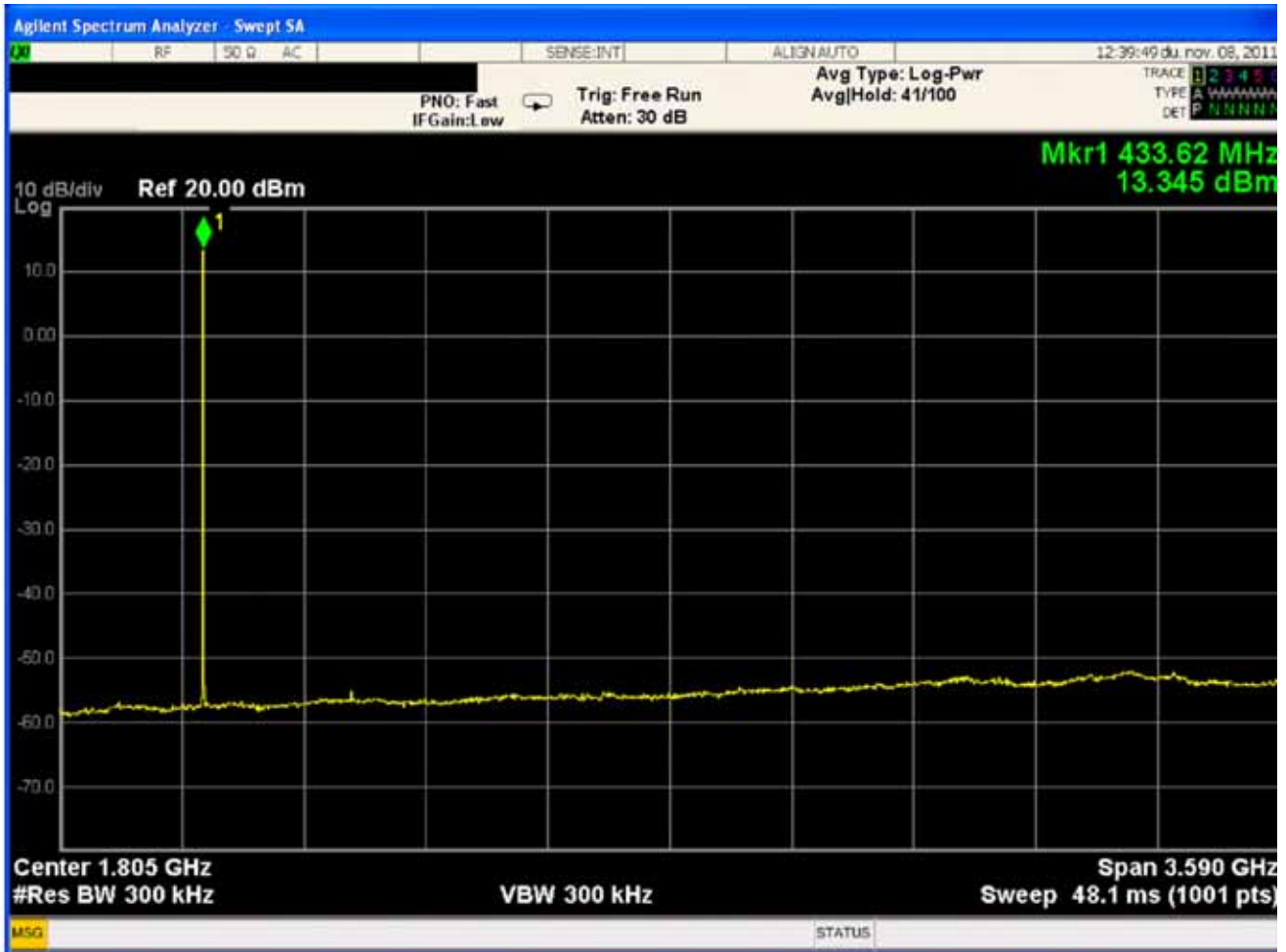
**Figure 29. Si4455 13 dBm Split TX/RX Board at 434 MHz with Wire-Wound Inductors, V$_{DD}$ = 3.2 V, DDAC[6:0] field in the PA_PWR_LVL Register is 3Fh, 22.7 mA**
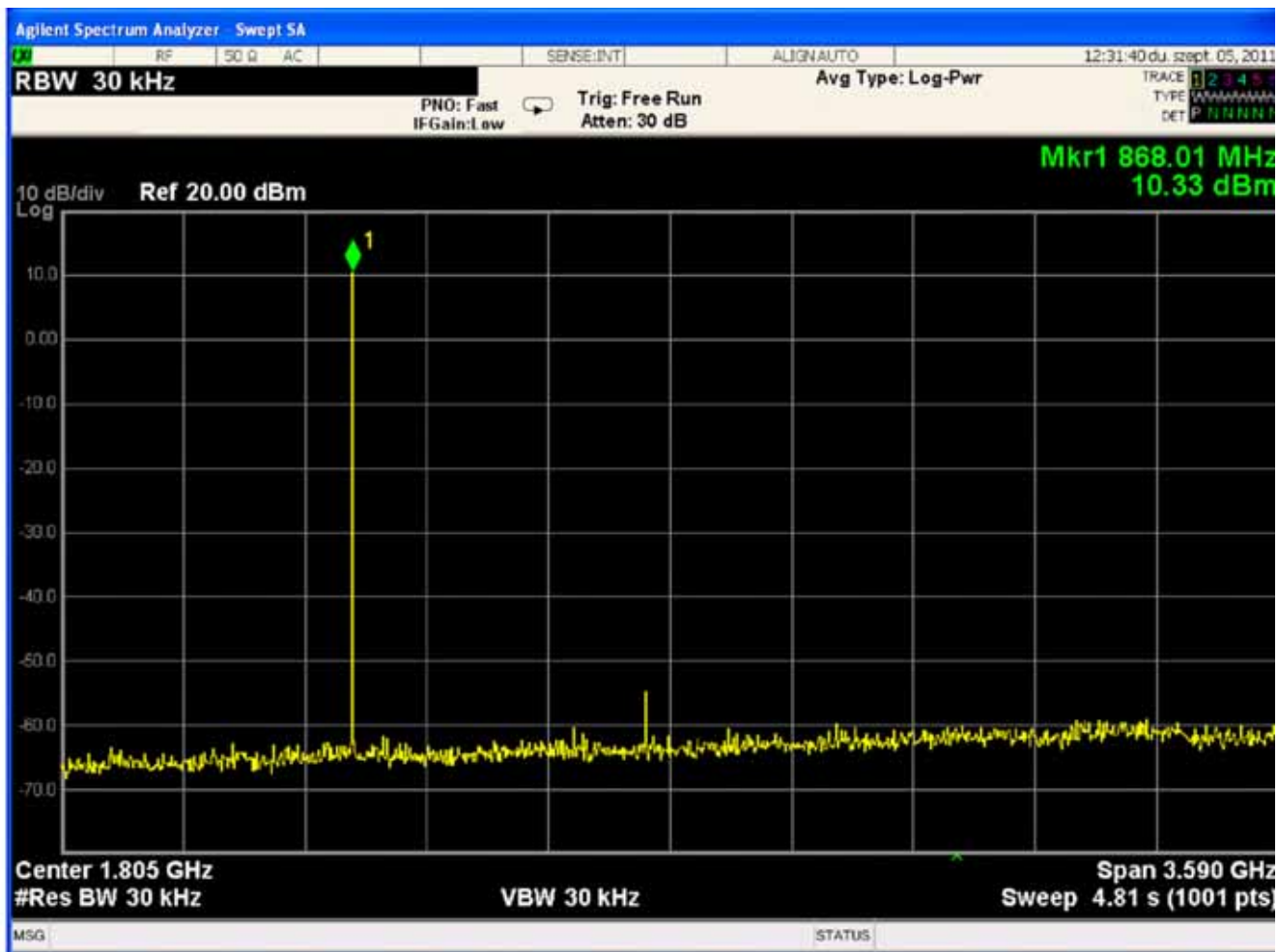
Figure 30. Si4455 10 dBm Split TX/RX Board at 868 MHz with Wire-Wound Inductors, V$_{DD}$ = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 19h, 16.4 mA
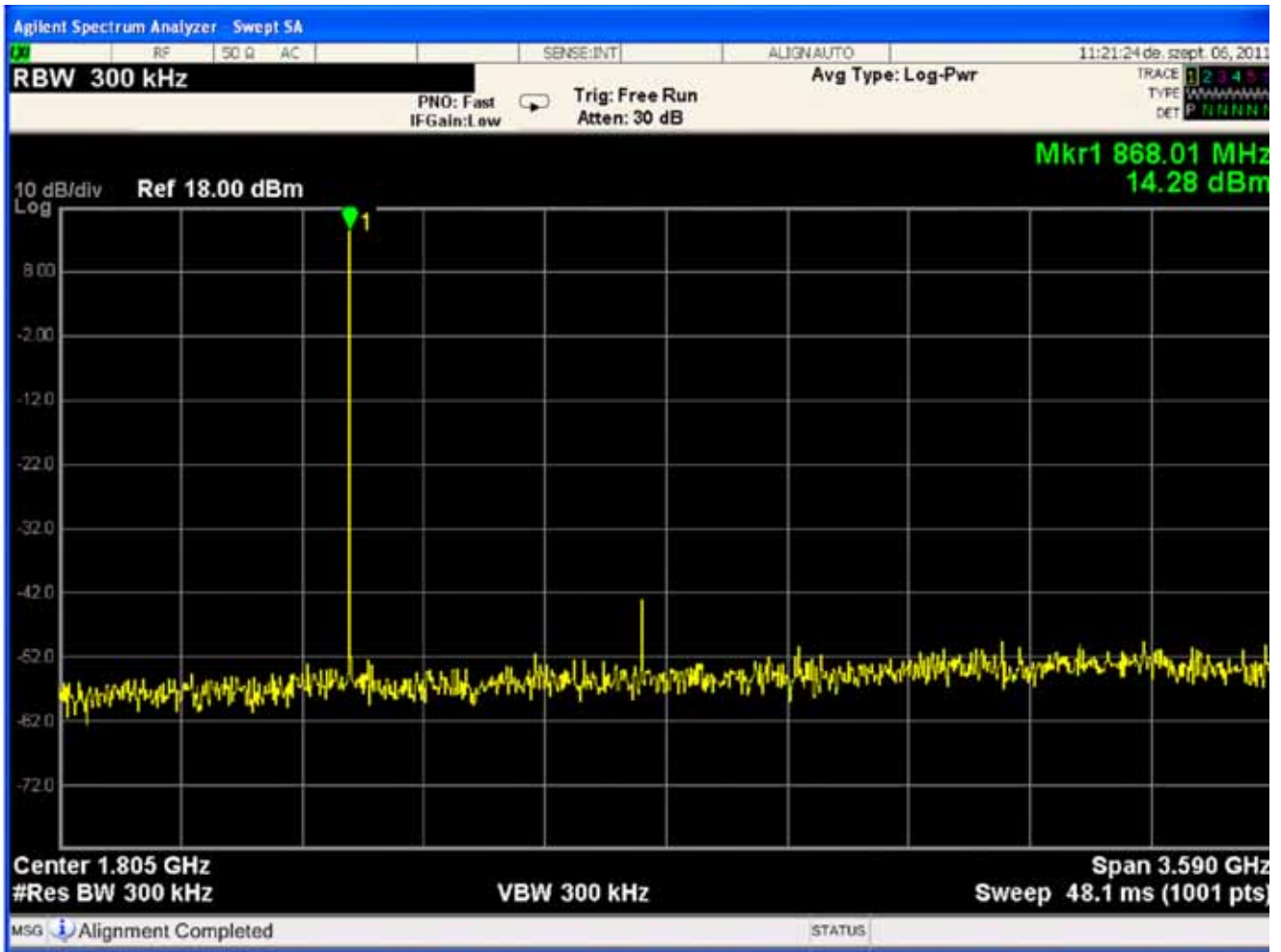
Figure 31. Si4455 14 dBm Split TX/RX Board at 868 MHz with Wire-Wound Inductors, V$_{DD}$ = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 3Dh, 24.8 mA

Si4455 Split TX/RX Board CLE Configurations with Multilayer Inductors

For 4455 Multilayer split TX/RX boards pls. use the TX part of the DT multilayer matches. The resulting spectrum plots are very close to those given for the multilayer DT boards in TX mode (see the multilayer inductor DT match plots at the beginning of this appendix).

Si4455 Direct Tie TX/RX Board CLE Configurations with Wire-Wound Inductors
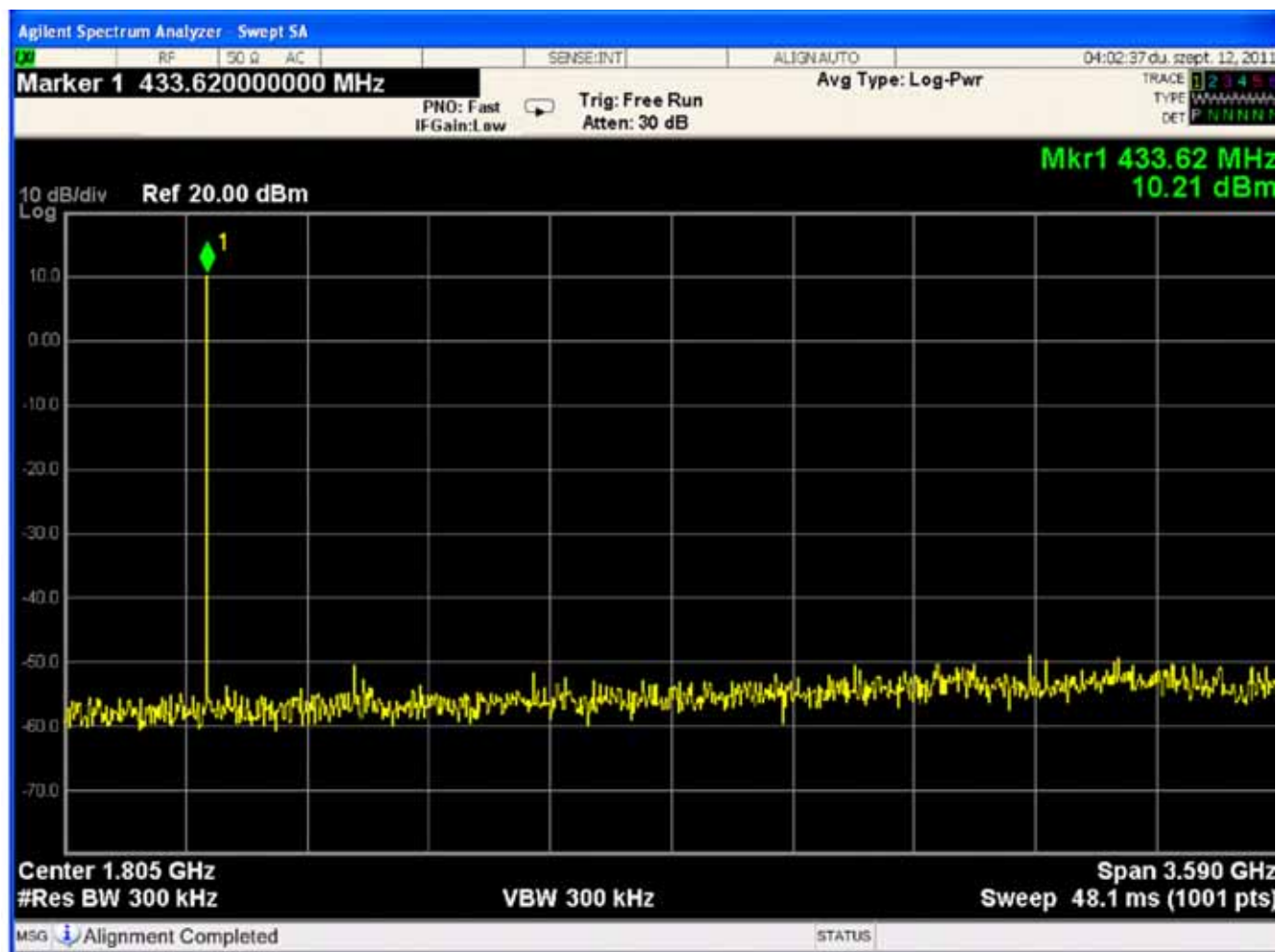
Figure 32. Si4455 10 dBm direct tie TX/RX Board at 434 MHz with Wire-Wound Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 1Ah, 16.9 mA
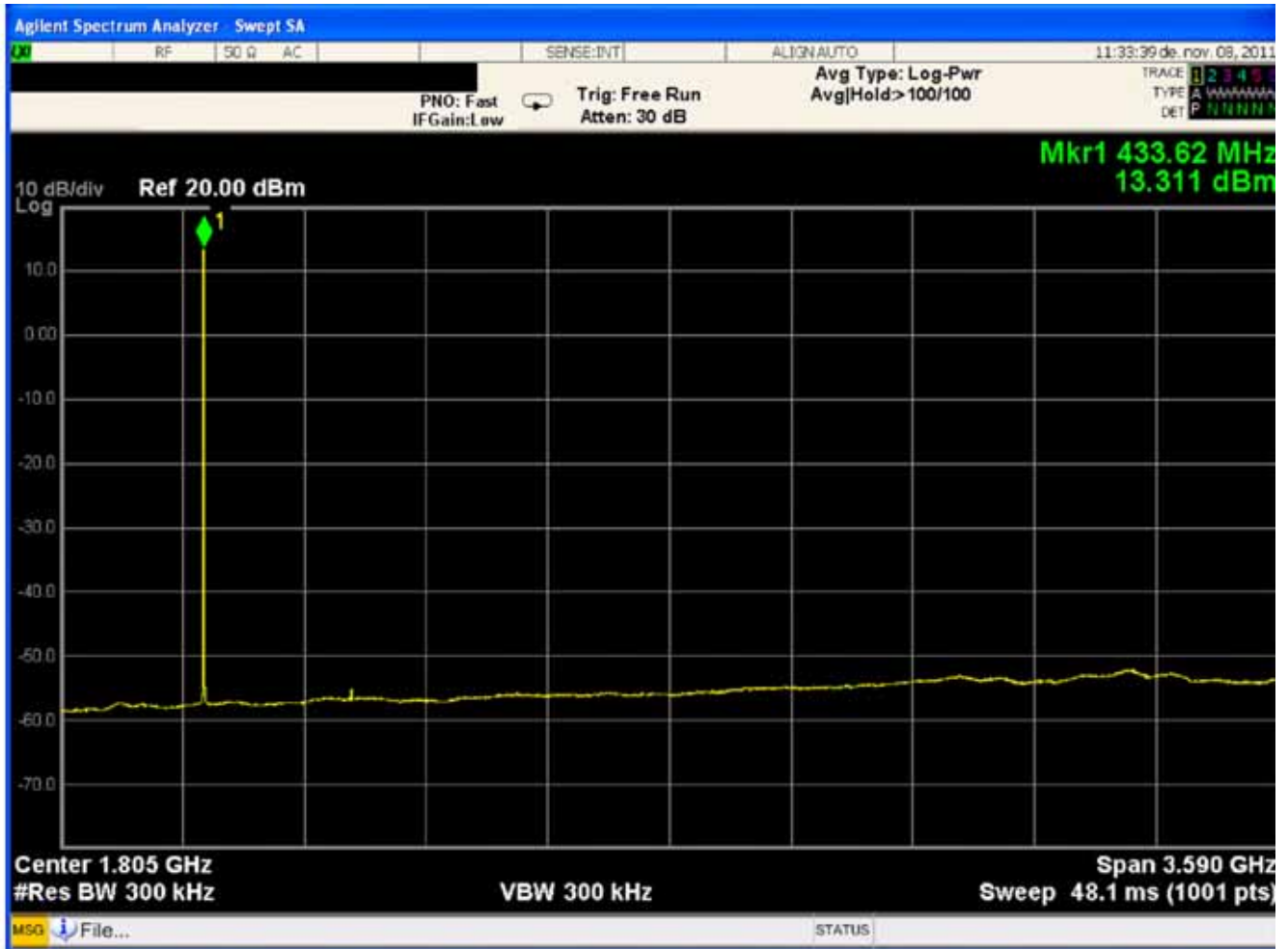
Figure 33. Si4455 13 dBm Direct Tie TX/RX Board at 434 MHz with Wire-Wound Inductors, V$_{DD}$ = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 3Fh, 23 mA
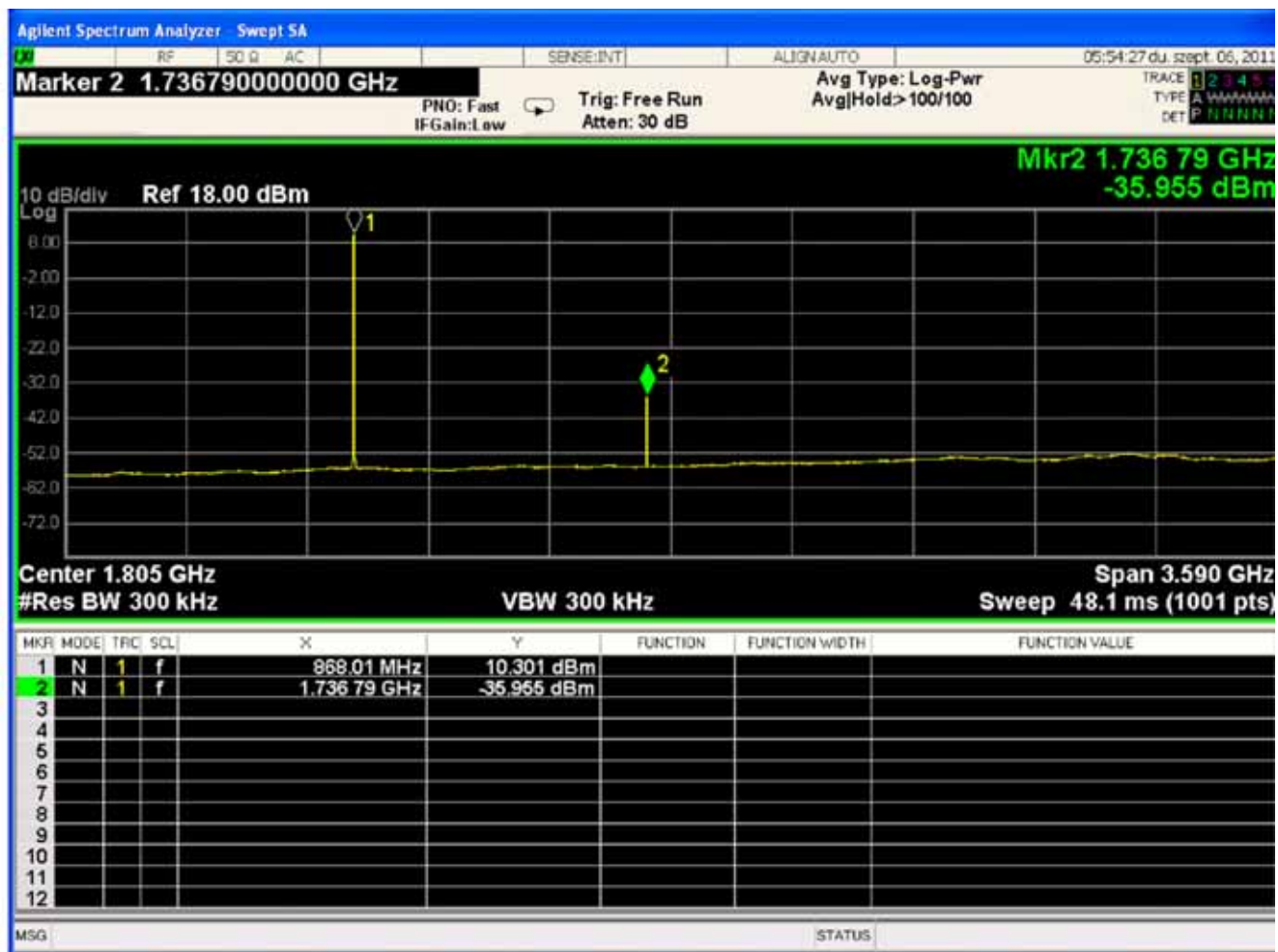
Figure 34. Si4455 10 dBm Direct Tie TX/RX Board at 868 MHz with Wire-Wound Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 18h, 17 mA
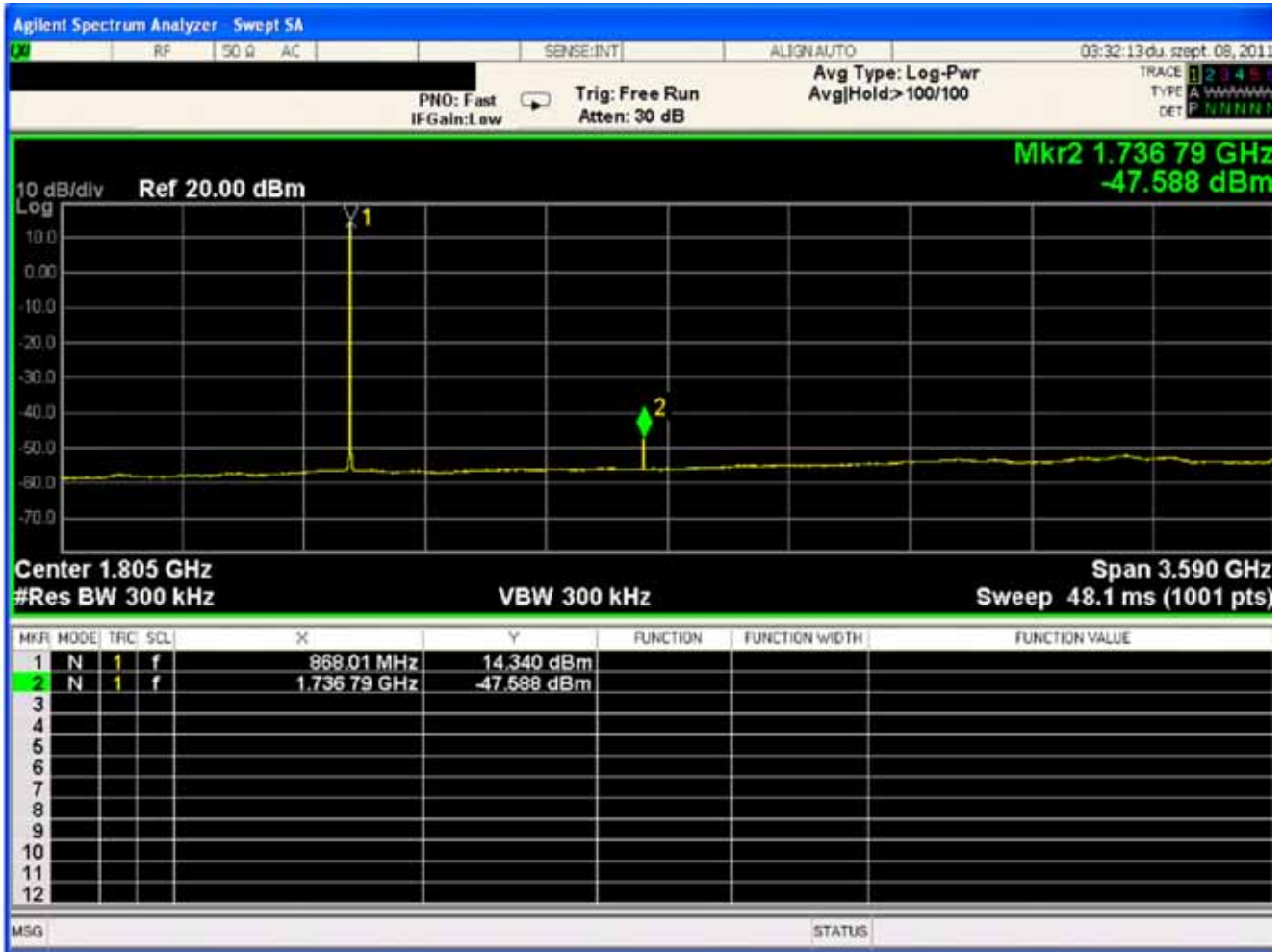
Figure 35. Si4455 14 dBm Direct Tie TX/RX Board at 868 MHz with Wire-Wound Inductors,
V_{DD} **= 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 44h, 25.6 mA**

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Si4455 Direct Tie TX/RX Board CLE Configurations with Multilayer Inductors
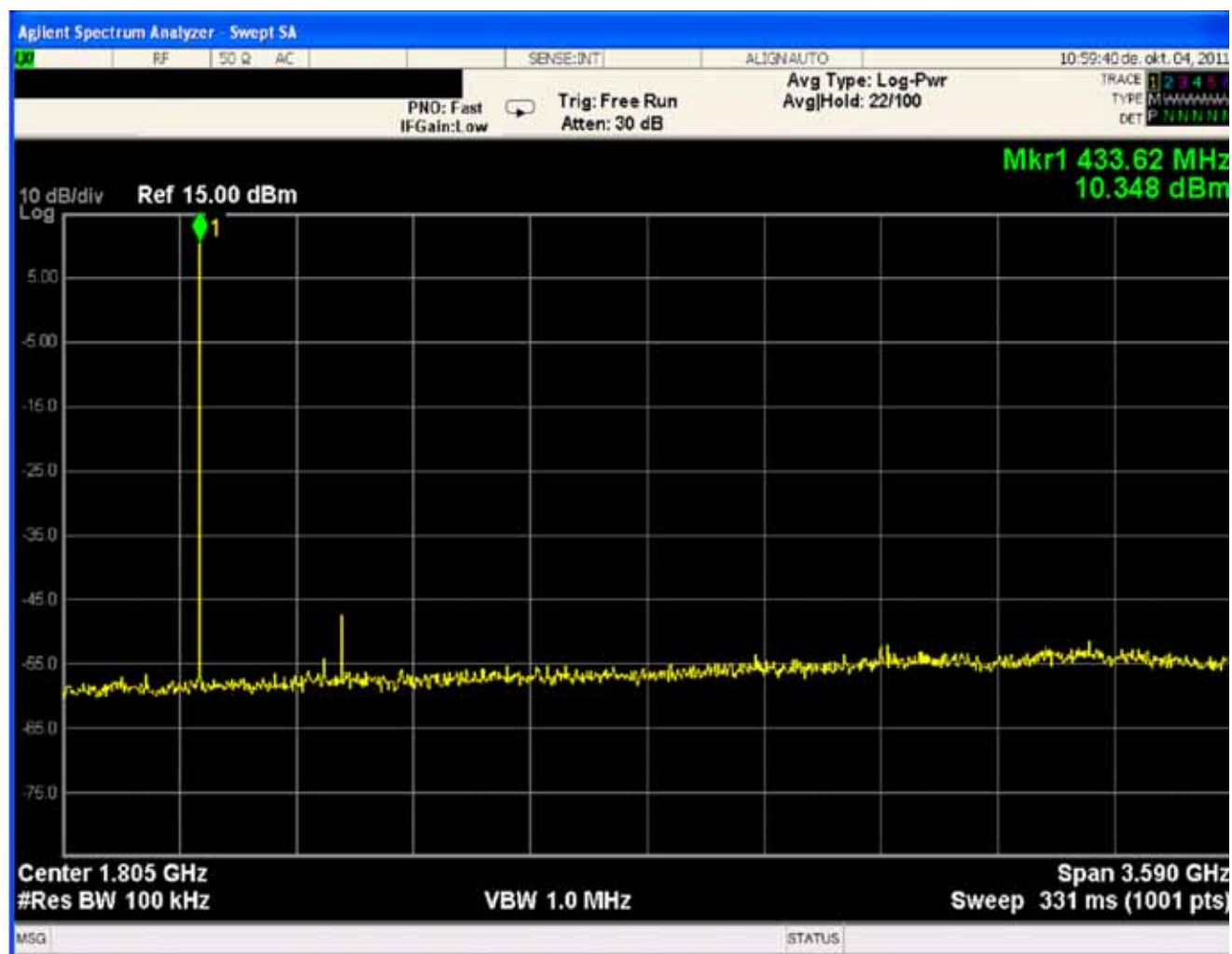
Figure 36. Si4455 10 dBm Direct Tie TX/RX Board at 434 MHz with Multilayer Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 2Ah, 17.1 mA
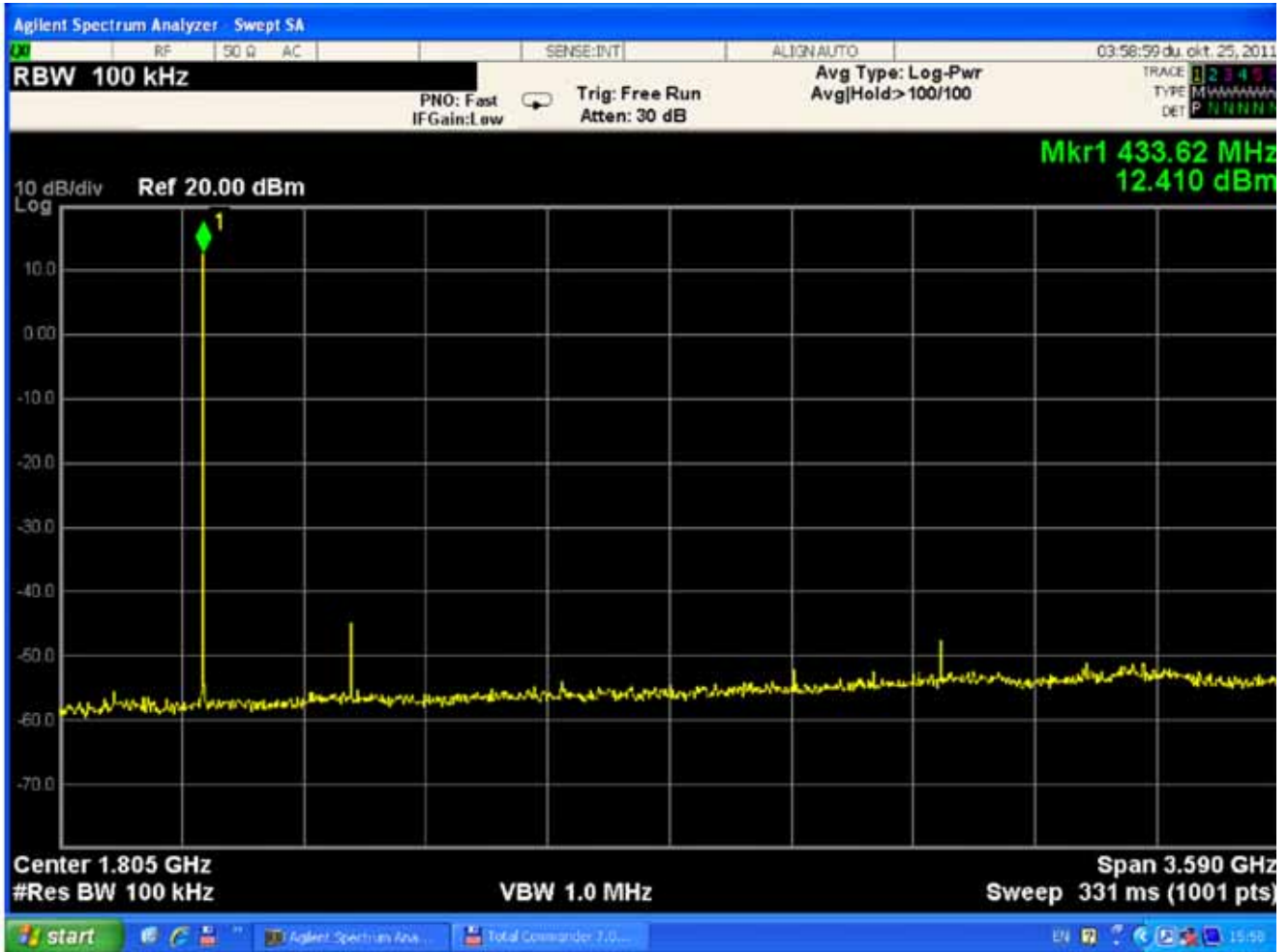
Figure 37. Si4455 12.3 dBm Direct Tie TX/RX Board at 434 MHz with Multilayer Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 4Fh, 23.1 mA
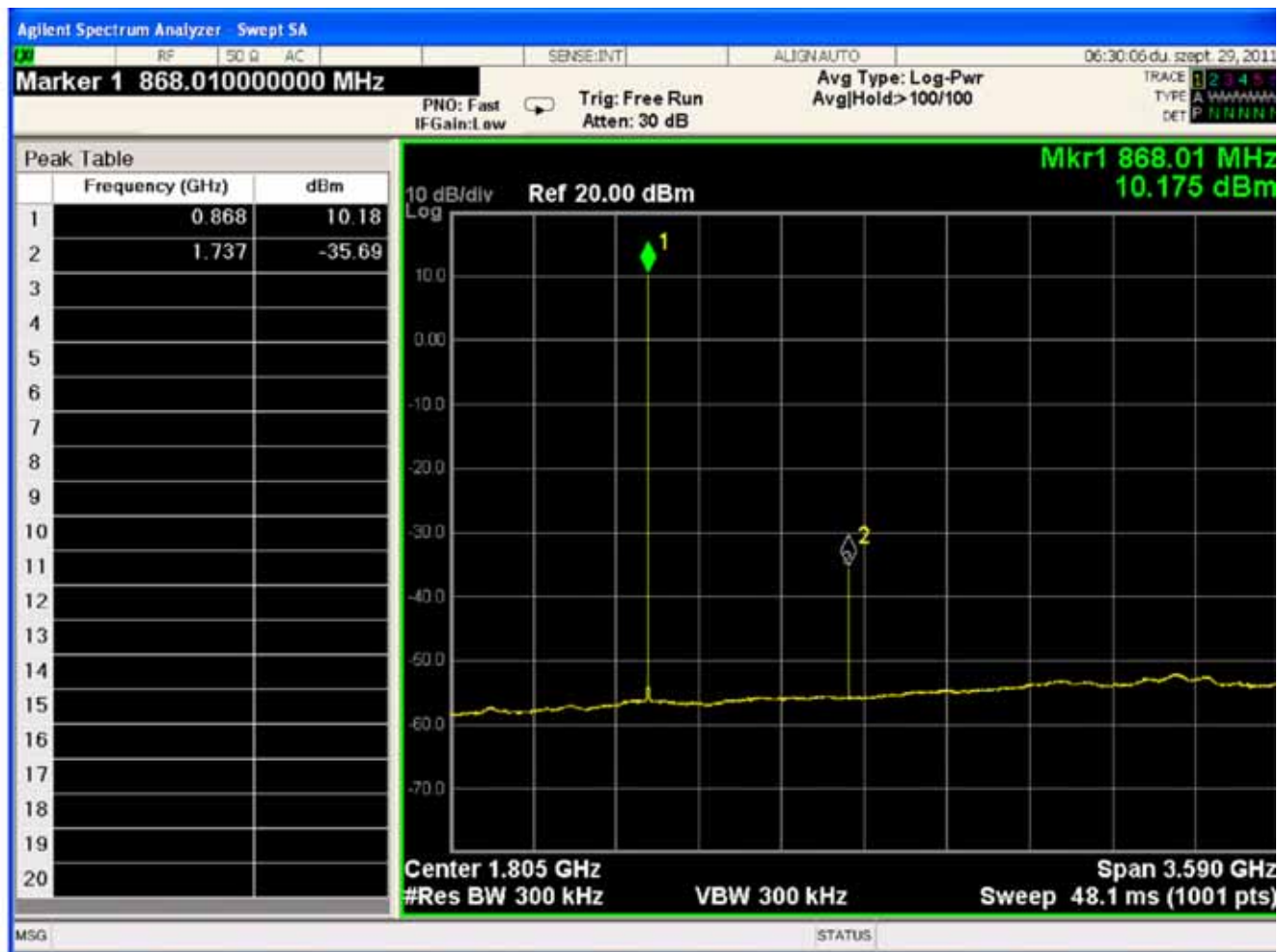
Figure 38. Si4455 10 dBm Direct Tie TX/RX Board at 868 MHz with Multilayer Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 21h, 19.3 mA
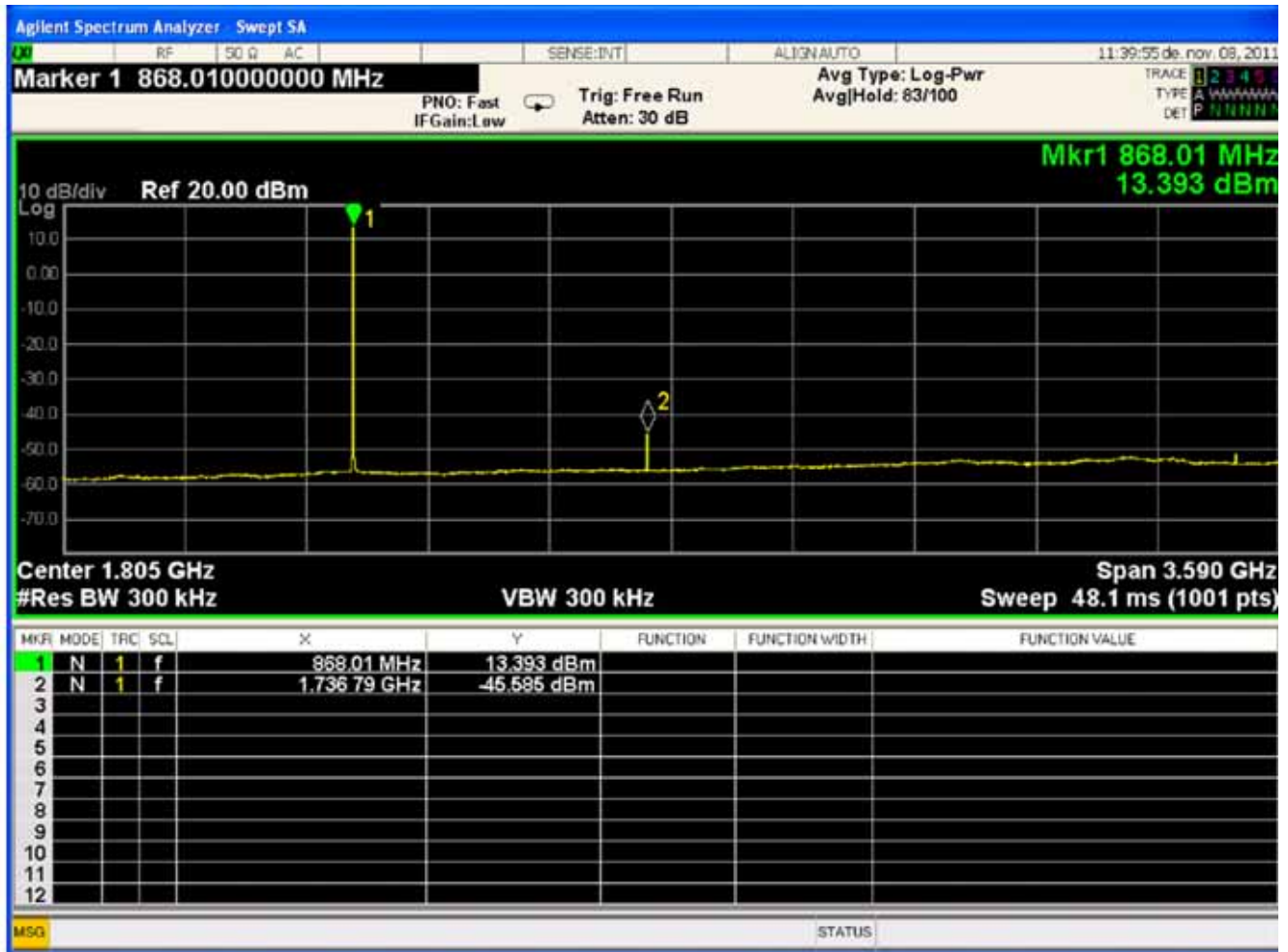
Figure 39. Si4455 13 dBm Direct Tie TX/RX Board at 868 MHz with Multilayer Inductors, V_{DD} = 3.2V, DDAC[6:0] Field in the PA_PWR_LVL Register is 3Ch, 24.1 mA

DOCUMENT CHANGE LIST

Revision 0.2 to Revision 0.3

- 'AN643: Si446x' changed to 'AN643: Si446x/Si4362'.
- Bug fixing.

Revision 0.3 to Revision 0.4

- Updated element values in tables.
- Updated table and figure numbers.
- Updated figures.

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