



# WGM160P Wi-Fi<sup>®</sup> Module Data Sheet

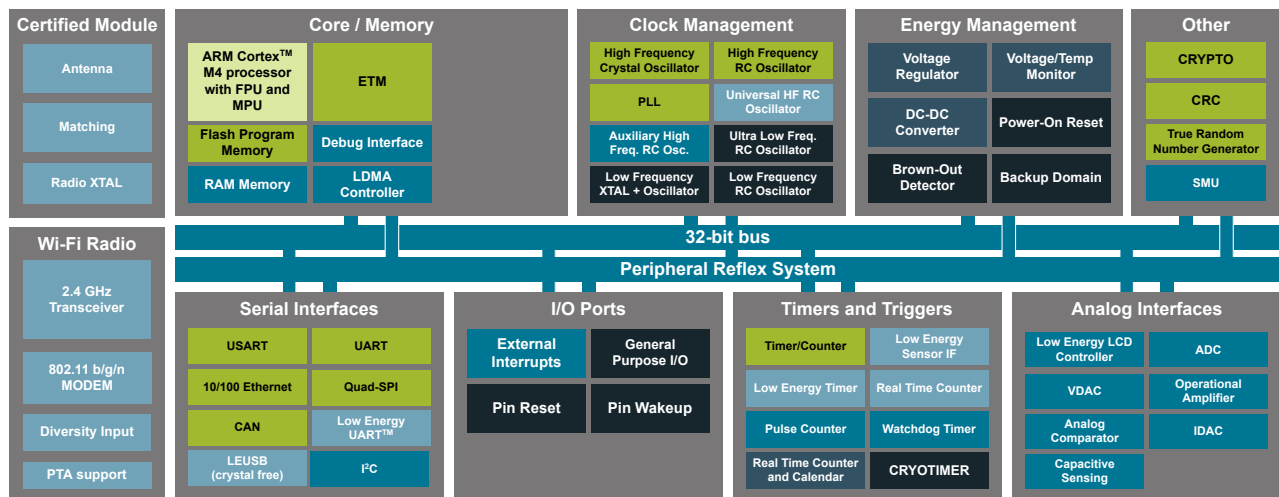
The WGM160P is an ultra low power standalone Wi-Fi<sup>®</sup> module targeted for applications requiring superior RF performance in noisy environments, low power consumption, high security, integrated customer applications and fast time to market.

The WGM160P module integrates all of the necessary elements required for a cloud connected IoT Wi-Fi application, including 802.11b/g/n radio, integrated chip antenna, certifications, microcontroller, Wi-Fi and IP stacks, HTTP server, and multiple protocols, such as TCP and UDP. Co-existence with external 2.4GHz transceivers is supported.

WGM160P can be configured to concurrently act as a Wi-Fi client and a Wi-Fi access point, which is ideal for user friendly device provisioning. WGM160P can natively host C- applications, removing the need for an external host controller. Alternatively, the Wi-Fi Module can run in Network Co-Processor (NCP) mode, leaving the complexity of TCP/IP networking to the module so that the customer's own host controller can be fully dedicated to processing the customer application tasks. The WGM160P module has highly flexible host and peripheral hardware interfaces for wide application use.

## KEY POINTS

- Available with integrated chip antenna or an RF pin
- Antenna diversity supported via secondary RF pin
- IEEE 802.11 b/g/n compliant
- TX power: +16 dBm
- RX sensitivity: -95.5 dBm
- CPU core: 32-bit ARM<sup>®</sup> Cortex-M4
- Flash memory: 2 MB
- RAM: 512 kB
- Concurrent mode: Wi-Fi AP and STA
- Ultra low power consumption
- Modular certification
  - CE, UKCA, FCC, ISED
  - MIC, KC
- End-to-end security
- Built-in 10/100 Ethernet Support
- Size: 23.8 mm x 14.2 mm x 2.3 mm



## 1. Key Features

The key features of the WGM160P module are listed below.

### Radio Features

- Built-in Antenna (optional)
- TX Power: +16 dBm
- RX Sensitivity: -95.5 dBm
- Superior blocking performance

### Wi-Fi Features

- 802.11: b/g/n
- Bit rate: up to 72.2 Mbps
- 802.11 Security: WPA2/WPA Personal
- STA (Station Mode)
- SoftAP (Soft Access Point Mode)

### Electrical Characteristics

- Supply voltage: 3.0V to 3.6V

### Environmental Specifications

- Temperature range: -40°C to +85°C

### Modular Certification

- CE and UKCA - EU and UK
- FCC - USA
- ISED - Canada
- MIC - Japan
- KC - South Korea
- RoHS/REACH compliant

### Dimensions

- L x W x H: 23.8 mm x 14.2 mm x 2.3 mm

### MCU Features

- ARM® Cortex-M4, 72MHz
- 512 kB RAM
- 2 MB Flash

### Hardware Interfaces

- Host interface: UART/SPI/USB
- Peripheral interfaces
  - 2 x USART (UART/SPI/I2S)
  - QSPI with Execute In Place (XIP) support
  - SD Card support (SPI)
  - Capacitive Touch Sensing in all GPIOs
  - LESENSE
  - 10/100 Ethernet MAC with RMI interface
  - USB device (2.0 Full speed)
  - I<sup>2</sup>C peripheral interfaces
  - CAN
- Up to 31 x GPIO with interrupts
- 2 x 12-bit ADC
- 2 x 12-bit DAC
- Rich selection of timers, inc. Real-time counters
- Co-existence interface (PTA: 2, 3, 4 wire)

## 2. Ordering Information

### Part Revisions

**Revision 3** of the WGM160P modules comes with Gecko OS kernel preloaded in the flash. **Those part are not recommended for new design (NRND) as Gecko OS has been set in maintenance mode and will turn End Of Life.** These parts can be used with the Full MAC software, but this requires changing the bootloader to erase the Gecko OS Kernel. Devices ship with the debug interface locked. Devices may be reprogrammed via serial or OTA DFU and preserve the device credentials. Unlocking the debug interface will result in loss of pre-programmed firmware, including Gecko OS Kernel and device credentials.

**Revision 4** of the WGM160P modules is recommended for new designs based on Full MAC software. Unlike revision 3, revision 4 parts do not have the Gecko OS kernel loaded, so there is no need to remove it before loading a FMAC based application. Devices ship with the debug interface unlocked.

All parts share the same characteristics regarding parameters below:

- Protocol: Wi-Fi (802.11 b/g/n)
- Max Tx Power: 16 dBm
- GPIO: up to 31
- 2048 Flash/512 Ram (kB)

| Part Number     | Status          | LFXTAL   | Antenna           | Pre-loaded Firmware       | Carrier  |
|-----------------|-----------------|----------|-------------------|---------------------------|----------|
| WGM160PX22KGA4  | Full Production | Included | Built-in          | Standard Gecko bootloader | Cut Tape |
| WGM160PX22KGA4R | Full Production | Included | Built-in          | Standard Gecko bootloader | Reel     |
| WGM160P022KGA4  | Full Production | None     | Built-in          | Standard Gecko bootloader | Cut Tape |
| WGM160P022KGA4R | Full Production | None     | Built-in          | Standard Gecko bootloader | Reel     |
| WGM160PX22KGN4  | Full Production | Included | External (RF Pin) | Standard Gecko bootloader | Cut Tape |
| WGM160PX22KGN4R | Full Production | Included | External (RF Pin) | Standard Gecko bootloader | Reel     |
| WGM160P022KGN4  | Full Production | None     | External (RF Pin) | Standard Gecko bootloader | Cut Tape |
| WGM160P022KGN4R | Full Production | None     | External (RF Pin) | Standard Gecko bootloader | Reel     |
| WGM160PX22KGA3  | <b>NRND</b>     | Included | Built-in          | Gecko OS kernel           | Cut Tape |
| WGM160PX22KGA3R | <b>NRND</b>     | Included | Built-in          | Gecko OS kernel           | Reel     |
| WGM160P022KGA3  | <b>NRND</b>     | None     | Built-in          | Gecko OS kernel           | Cut Tape |
| WGM160P022KGA3R | <b>NRND</b>     | None     | Built-in          | Gecko OS kernel           | Reel     |
| WGM160PX22KGN3  | <b>NRND</b>     | Included | External (RF Pin) | Gecko OS kernel           | Cut Tape |
| WGM160PX22KGN3R | <b>NRND</b>     | Included | External (RF Pin) | Gecko OS kernel           | Reel     |
| WGM160P022KGN3  | <b>NRND</b>     | None     | External (RF Pin) | Gecko OS kernel           | Cut Tape |
| WGM160P022KGN3R | <b>NRND</b>     | None     | External (RF Pin) | Gecko OS kernel           | Reel     |

**Note:**

1. SLWSTK6121A Wireless Starter Kit and SLWRB4321A Radio Board are available to start developing with WGM160P Wi-Fi modules.
2. Devices listed may be referred to by the product family name (WGM160P), model name (WGM160P22A / WGM160P22N) or the full orderable part number throughout this document.

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### 3. System Overview

#### 3.1 Introduction

The WGM160P module combines the WF200 Wi-Fi transceiver with an EFM32GG11 microcontroller to deliver a complete and certified standalone Wi-Fi solution, with the ability to run customer application on an Cortex M4 processor.

For more details on the software platform, please consult our [online documentation](#).

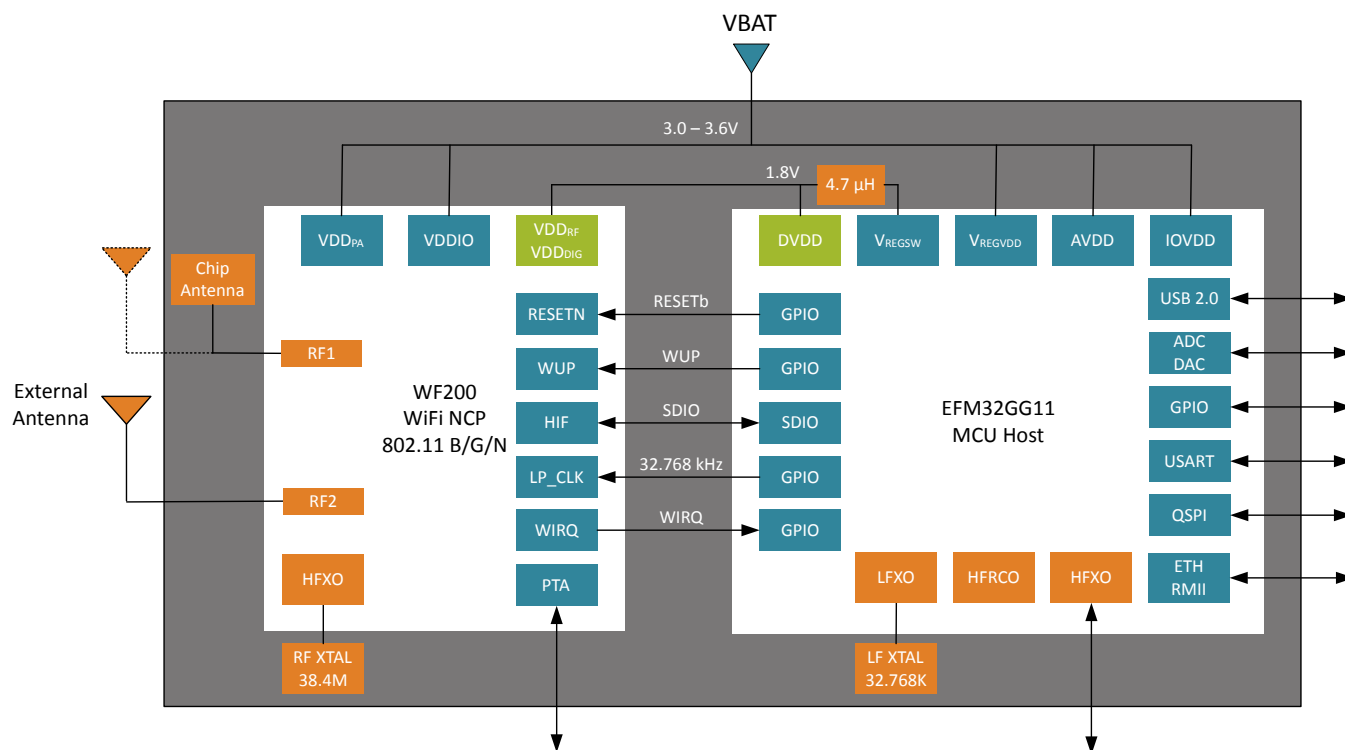


Figure 3.1. WGM160P Block Diagram

#### 3.2 Wi-Fi Supported 2.4 GHz ISM Modulations, BW, and Channels

Table 3.1. Supported Wi-Fi Modulations, BW, and Channels

| Parameter                | Symbol | Test Condition               | Min  | Typ  | Max               | Unit |
|--------------------------|--------|------------------------------|------|------|-------------------|------|
| Channel Center Frequency | CHAN   | Subject to Regulatory Agency | 2412 | 2437 | 2484 <sup>1</sup> | MHz  |
| Channel Bandwidth        | BW     |                              | —    | 20   | —                 | MHz  |

**Note:**  
1. Channel 14 only supports 1 and 2 Mbps modulations.

## 4. Electrical Specifications

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on  $T_{AMB} = 25\text{ °C}$ ;  $V_{VBAT} = 3.3\text{V}$ ; Center Frequency = 2,437 MHz.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a 50  $\Omega$  antenna port. Conducted RF measurements include additional output power reductions to guarantee WiFi and regulatory emissions compliance while connected to the specified antennas which have non-ideal impedance loading.

Refer to Section 4.2 [Operating Conditions](#) for more details about operational supply and temperature limits.

### 4.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at <http://www.silabs.com/support/quality/pages/default.aspx>.

**Table 4.1. Absolute Maximum Ratings**

| Parameter   | Symbol             | Test Condition  | Min  | Typ | Max                     | Unit |
|---|--------------------|---|------|-----|-------------------------|------|
| Storage temperature                                   | $T_{STG}$          |   | -40  | —   | 105                     | °C   |
| RF power level at RF1 and RF2 ports                   | $P_{RFMAX}$        | Max power that can be applied to input of recommended matching network connected to RF1 and RF2 pins. | —    | —   | 10                      | dBm  |
| Maximum supply voltage to VBAT                        | $V_{BATMAX}$       |   | -0.3 | —   | 3.6                     | V    |
| DC voltage on I/O pins                                | $V_{GMAX}$         | 5 V tolerant GPIO (PF0, PF1, PF10, PF11) <sup>1 2</sup>   | -0.3 | —   | Min of 5.25 and VBAT +2 | V    |
|   |                    | All other GPIO and PTA pins   | -0.3 | —   | $V_{BAT} + 0.3$         | V    |
| Current into any GPIO pin                             | $I_{O_{MAX}}$      |   | —    | —   | 20                      | mA   |
| Sum of current into all GPIO pins                     | $I_{O_{ALL\_MAX}}$ |   | —    | —   | 150                     | mA   |
| Range of load impedance at RF1 and RF2 pins during TX | $LOAD_{TX}$        |   | —    | —   | 10:1                    | VSWR |

**Note:**

1. When a GPIO is used for analog functions via the APORT, the maximum voltage is VBAT.
2. To operate above the VBAT supply rail, over-voltage tolerance must be enabled according to the GPIO\_Px\_OVTDIS register. Pins with over-voltage tolerance disabled have the same limits as all other GPIO (max = VBAT + 0.3 V).

## 4.2 Operating Conditions

**Table 4.2. Recommended Operating Conditions**

| Parameter                                   | Symbol     | Test Condition | Min | Typ | Max | Unit |
|---|------------|----------------|-----|-----|-----|------|
| Ambient operating temperature               | $T_A$      |                | -40 | —   | 85  | °C   |
| Nominal supply voltage to VBAT <sup>1</sup> | $V_{VBAT}$ |                | 3.0 | 3.3 | 3.6 | V    |

**Note:**

- Operating outside of the recommended voltage supply range is not supported. The module may disable WiFi transmit functions when operating outside of this range in order to guarantee regulatory emissions compliance.

## 4.3 Power Consumption

All currents measured with VBAT = 3.3 V.

**Table 4.3. Power Consumption**

| Parameter  | Symbol             | Test Condition  | Min | Typ   | Max | Unit |
|--|--------------------|---|-----|-------|-----|------|
| Continuous TX current, 1 Mbps, max power setting | $I_{TX_{MAX}}$     |   | —   | 141.3 | —   | mA   |
| Continuous TX current, MCS7, max power setting   | $I_{TX_{MAX\_N}}$  |   | —   | 131.4 | —   | mA   |
| Continuous RX listen current                     | $I_{RX_{MAX}}$     |   | —   | 36.6  | —   | mA   |
| Continuous RX receive current, 1 Mbps            | $I_{RX_{MAXR}}$    |   | —   | 34.5  | —   | mA   |
| Continuous RX receive current, MCS7              | $I_{RX_{MAXR\_N}}$ |   | —   | 38.5  | —   | mA   |
| Average Current DTIM=1                           | $I_{LP\_DTIM1}$    | Connected as STATION. EFM32GG11 in EM2 mode. DC-DC in Low Noise mode CCM 3 MHz. | —   | 641   | —   | µA   |
| Average Current DTIM=3                           | $I_{LP\_DTIM3}$    | Connected as STATION. EFM32GG11 in EM2 mode. DC-DC in Low Noise mode CCM 3 MHz. | —   | 270   | —   | µA   |
| Average Current DTIM=10                          | $I_{LP\_DTIM10}$   | Connected as STATION. EFM32GG11 in EM2 mode. DC-DC in Low Noise mode CCM 3 MHz. | —   | 147   | —   | µA   |
| Sleep current                                    | $I_{SLEEP}$        | EFM32GG11 in EM2 mode, DC-DC in Low-Noise mode CCM 3 MHz.                       | —   | 90    | —   | µA   |
| Standby mode current                             | $I_{STANDBY}$      | No memory retained. WF200 in Shutdown mode, EFM32GG11 in EM4 mode.              | —   | 217   | —   | nA   |



## 4.4 Digital I/O Specifications

Table 4.4. Digital I/O Specifications

| Parameter  | Symbol            | Test Condition  | Min | Typ       | Max | Unit |
|--|-------------------|---|-----|-----------|-----|------|
| Voltage input high (relative to VBAT)                    | V <sub>IH</sub>   |   | 70  | —         | —   | %    |
| Voltage input low (relative to VBAT)                     | V <sub>IL</sub>   |   | —   | —         | 30  | %    |
| Logic low output voltage (relative to VBAT)              | V <sub>OL</sub>   | PTA Pins, Sinking 5 mA  | —   | —         | 25  | %    |
|  |                   | GPIO Pins, Sinking 20 mA, DRIVESTRENGTH = STRONG                              | —   | —         | 25  | %    |
| Logic high output voltage (relative to VBAT)             | V <sub>OH</sub>   | PTA Pins, Sourcing 5 mA   | 75  | —         | —   | %    |
|  |                   | GPIO Pins, Sourcing 20 mA, DRIVESTRENGTH = STRONG                             | 75  | —         | —   | %    |
| Input leakage current                                    | I <sub>Leak</sub> | All I/O when GPIO voltage ≤ VBAT  | —   | 1         | —   | nA   |
|  |                   | 5 V Tolerant I/O (PF0, PF1, PF10, PF11) when VBAT < GPIO voltage ≤ VBAT + 2 V | —   | 3.3       | 15  | μA   |
| Pullup resistance  | R <sub>PU</sub>   |   | 30  | 40        | 65  | kΩ   |
| Pulldown resistance                                      | R <sub>PD</sub>   |   | 30  | 40        | 65  | kΩ   |
| Output fall time from V <sub>OH</sub> to V <sub>OL</sub> | T <sub>OF</sub>   | 50 pF load, DRIVESTRENGTH = STRONG, SLEWRATE = 0x6                            | —   | 1.8       | —   | ns   |
|  |                   | 50 pF load, DRIVESTRENGTH = WEAK, SLEWRATE = 0x6                              | —   | 4.5       | —   | ns   |
| Output rise time from V <sub>OL</sub> to V <sub>OH</sub> | T <sub>OR</sub>   | 50 pF load, DRIVESTRENGTH = STRONG, SLEWRATE = 0x6                            | —   | 2.2       | —   | ns   |
|  |                   | 50 pF load, DRIVESTRENGTH = WEAK, SLEWRATE = 0x6                              | —   | 7.4       | —   | ns   |
| Required external series resistor on USB D+ and D-       | R <sub>USB</sub>  |   | —   | 33 +/-10% | —   | Ω    |

#### 4.5 RF Transmitter General Characteristics

Unless otherwise indicated, typical conditions are: Operating Ambient Temp = 25 °C, VBAT = 3.3 V, center frequency = 2,437 MHz, and measured in 50 Ω test equipment attached at antenna port.

Measurements for this specification are made at the 50 Ω Antenna Port. See Section 5.1.1 [Antenna Ports](#). Conducted RF measurements include additional output power reductions to guarantee WiFi and regulatory emissions compliance while connected to the specified antennas which have non-ideal impedance loading.

**Table 4.5. RF Transmitter Characteristics**

| Parameter   | Symbol                       | Test Condition     | Min | Typ         | Max | Unit |
|---|------------------------------|--------------------|-----|-------------|-----|------|
| Maximum RMS Output Power at Antenna (High Power PA) <sup>1</sup>      | POUT <sub>MAX_RMS_HPPA</sub> | 802.11b: 1 Mbps    | —   | 16.1        | —   | dBm  |
|   |                              | 802.11b: 11 Mbps   | —   | 15.1        | —   | dBm  |
|   |                              | 802.11g: 6 Mbps    | —   | 14.7        | —   | dBm  |
|   |                              | 802.11g: 54 Mbps   | —   | 9.1         | —   | dBm  |
|   |                              | 802.11n: MCS=0     | —   | 14.4        | —   | dBm  |
|   |                              | 802.11n: MCS=7     | —   | 5.8         | —   | dBm  |
| Carrier frequency error   | CARR <sub>FREQ_ERROR</sub>   | Across temperature | -25 | —           | 25  | ppm  |
| POUT variation over supply voltage range, relative to nominal 3.3 V   | POUT <sub>VAR_V</sub>        | VBAT = 3.0-3.6 V   | —   | +0.3 / -1.1 | —   | dB   |
| POUT variation over frequency range, relative to average <sup>1</sup> | POUT <sub>VAR_F</sub>        | CH1 to CH14        | —   | +/-0.15     | —   | dB   |
| POUT variation over temperature range, relative to 25C                | POUT <sub>VAR_T</sub>        | -40 to +85C        | —   | +0.1 / -1.2 | —   | dB   |

**Note:**

1. Rated power levels may not apply to the edge channels, which may need additional backoff for FCC compliance.

#### 4.6 RF Receiver General Characteristics

Unless otherwise indicated, typical conditions are: Operating Ambient Temp = 25 °C, VBAT = 3.3 V, center frequency = 2,437 MHz, and measured in 50 Ω test equipment attached at antenna port.

Measurements for this specification are made at the 50 Ω Antenna Port. See Section 5.1.1 Antenna Ports.

**Table 4.6. RF Receiver Characteristics**

| Parameter   | Symbol                   | Test Condition   | Min | Typ    | Max | Unit |
|---|--------------------------|------------------|-----|--------|-----|------|
| RX Sensitivity for 8% FER (1024 Octet) <sup>1</sup>       | SENS <sub>B</sub>        | 802.11b: 1 Mbps  | —   | -95.5  | —   | dBm  |
|   |                          | 802.11b: 11 Mbps | —   | -88.3  | —   | dBm  |
| RX Sensitivity for 10% PER (1024 Octet) <sup>1</sup>      | SENS <sub>G</sub>        | 802.11g: 6 Mbps  | —   | -89    | —   | dBm  |
|   |                          | 802.11g: 54 Mbps | —   | -75.2  | —   | dBm  |
| RX Sensitivity for 10% PER (4096 Octet) <sup>1</sup>      | SENSE <sub>N</sub>       | 802.11n: MCS=0   | —   | -89.3  | —   | dBm  |
|   |                          | 802.11n: MCS=7   | —   | -72.8  | —   | dBm  |
| RX Max Strong Signal for 8% FER (1024 Octet)              | RX <sub>SAT_B</sub>      | 802.11b: 1 Mbps  | —   | -4.0   | —   | dBm  |
|   |                          | 802.11b: 11 Mbps | —   | -10.0  | —   | dBm  |
| RX Max Strong Signal for 10% PER (1024 Octet)             | RX <sub>SAT_G</sub>      | 802.11g: 6 Mbps  | —   | -9.0   | —   | dBm  |
|   |                          | 802.11g: 54 Mbps | —   | -9.0   | —   | dBm  |
| RX Max Strong Signal for 10% PER (4096 Octet)             | RX <sub>SAT_N</sub>      | 802.11n: MCS=0   | —   | -9.0   | —   | dBm  |
|   |                          | 802.11n: MCS=7   | —   | -9.0   | —   | dBm  |
| Sensitivity variation across frequency range, CH1 to CH14 | SENS <sub>VAR_V</sub>    | 802.11b 1 Mbps   | —   | +/-0.5 | —   | dB   |
| Sensitivity variation over temperature range, -40 to 85C  | SENS <sub>VAR_TEMP</sub> | 802.11b 1 Mbps   | —   | +/-1.3 | —   | dB   |
| RX Channel power Indicator Step Size                      | RCPI <sub>STEP</sub>     | 802.11b: 1 Mbps  | —   | 0.5    | —   | dB   |

**Note:**

1. Measurement taken at U.FL connector. Includes 0.5 dB loss introduced by connector.

#### 4.7 Radiated Characteristics

Unless otherwise indicated, typical conditions are: Operating Ambient Temp = 25 °C, VBAT = 3.3 V, center frequency = 2437 MHz, using the integrated antenna, and measured with the ideal application board size for 2.4 GHz radiation.

**Table 4.7. Radiated Characteristics**

| Parameter  | Symbol              | Test Condition                   | Min | Typ  | Max | Unit |
|--|---------------------|----------------------------------|-----|------|-----|------|
| Application board size, radiated edge "X" dimension <sup>1</sup> | PCB <sub>X_MM</sub> |                                  | 40  | 50   | —   | mm   |
| Antenna Efficiency   | ANT <sub>EFF</sub>  | Optimal application board design | —   | -1.4 | —   | dB   |

**Note:**

1. Refer to "UG384: WGM160P Hardware Design Users Guide" for more PCB layout details.

## 4.8 Microcontroller Peripherals

WGM160P offers an extensive list of peripherals, some of which are listed below:

- 12-bit ADC
- 12-bit DAC
- GPIO
- USART (UART/SPI/I2S)
- QSPI with Execute In Place (XIP) support
- Capacitive Touch Sensing in all GPIOs
- LESENSE
- 10/100 Ethernet MAC with RMI interface (50 MHz external crystal required)
- USB device (2.0 Full speed)
- I<sup>2</sup>C peripheral interfaces
- CAN
- Timers
- LCD Driver

For more information on the pins these peripherals are available on, please consult: [7.2 GPIO Functionality](#) and [7.3 Alternate Pin Functionality](#).

For details on the electrical performance of these peripherals, please consult the relevant portions of Section 4 in the [EFM32GG11 Family Datasheet](#) (See EFM32GG11B820F2048GM64).

## 5. Typical Applications and Connections

For more information, see [UG384: WGM160P Hardware Design Users Guide](#).

### 5.1 RF Connections

#### 5.1.1 Antenna Ports

The WGM160P offers two RF ports that support antenna diversity using an internal switch. In applications with only one antenna, the unused port should be terminated to ground with a 47-51  $\Omega$  resistor. Leaving the unused port floating or tying directly to ground will result in degraded performance. An external antenna connected to either RF port needs to be properly matched with at least -10dB return loss (VSWR < 2).

#### 5.1.2 Antenna Diversity

In applications where multipath fading is a potential issue, such as indoors, a second antenna can be connected. A firmware feature can be enabled to automatically determine which of the two antennas gives a better signal, allowing significant improvement in link reliability.

### 5.2 Multi-Protocol Coexistence

Packet Transmit Arbitration (PTA) pins are provide to share antenna and optimize coexistence performance with other networks including other protocols. See Application Notes [AN1128: Bluetooth Coexistence with Wi-Fi](#), [AN1017: Zigbee and Thread Coexistence with Wi-Fi](#) and [Wi-Fi Coexistence with Other 2.4GHz Radio Protocols](#) section in [www.docs.silabs.com/wifi](http://www.docs.silabs.com/wifi).

### 5.3 Example Schematic

**Note:** RF1 pin connected internally to module antenna in WGM160PX22KGAX.

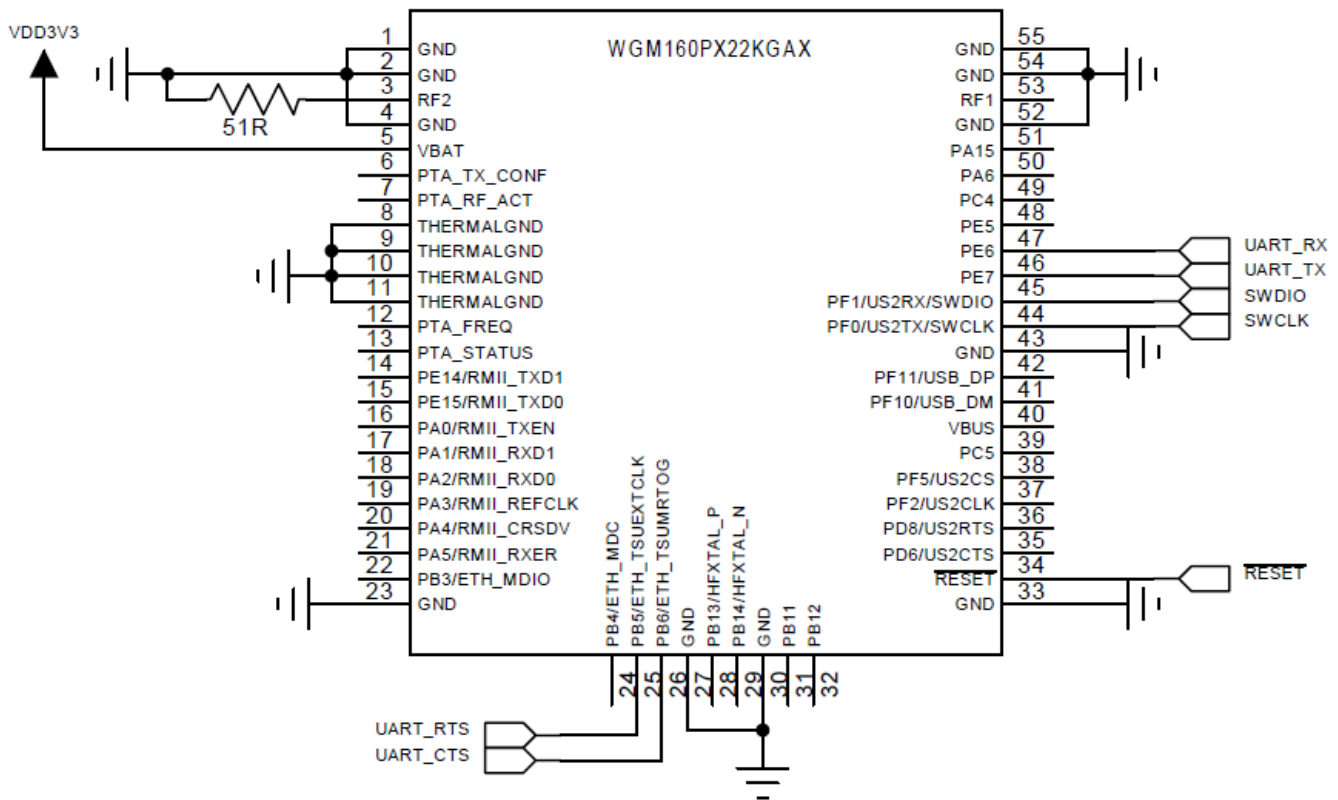


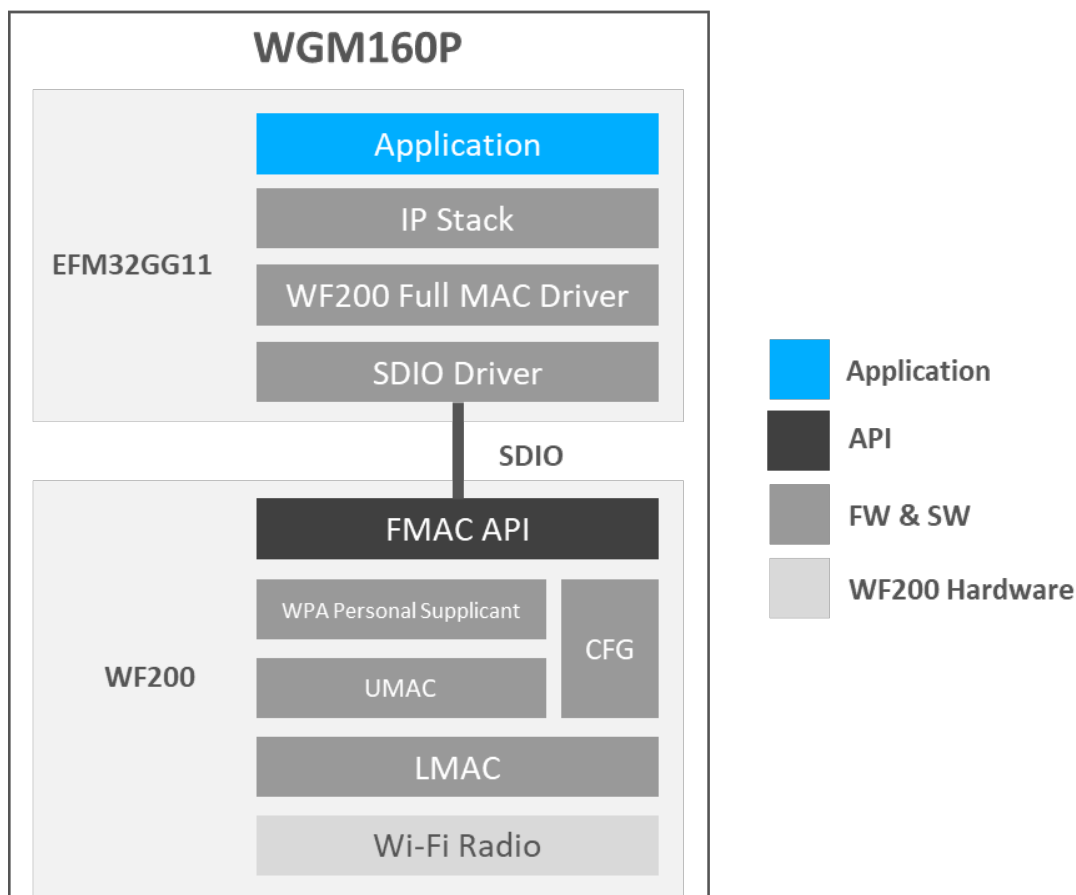
Figure 5.1. Example Schematic for NCP Application

## 6. Software

WGM160P software is based on the FMAC (Full MAC) driver. Architecture and examples are described below.

### 6.1 FMAC (Full MAC) Driver Architecture

Utilizing the Full MAC driver, both the lower MAC and upper MAC are running in WF200 of the WGM160P. The WF200 contains a WPA/WPA2 personal supplicant, allowing it to handle full MAC responsibilities without utilizing the host MCU. The host receives an IP packet and implements all stack layers necessary above it. The figure below shows the typical software architecture in Full MAC implementations.



**Figure 6.1. Full MAC Implementation**

**Note:** The WPA supplicant on WF200 does not support WPA enterprise. If WPA-enterprise is required, then it should be implemented above the IP stack in the EFM32GG11 software.

### 6.2 Examples

Numerous software examples are available from Simplicity Studio or the GitHub repository. These examples utilize the MicriumOS Kernel, FreeRTOS or Bare Metal (no RTOS). Unless otherwise specified in the repository, all examples are considered to be EXPERIMENTAL QUALITY which implies that the code provided in the repos has not been formally tested and is provided as-is. They are not suitable for production environment.

For more information see the following:

- <https://docs.silabs.com/wifi/>
- <https://github.com/SiliconLabs/wfx-fullMAC-tools>

## 7. Pin Descriptions

### 7.1 WGM160P Device Pinout

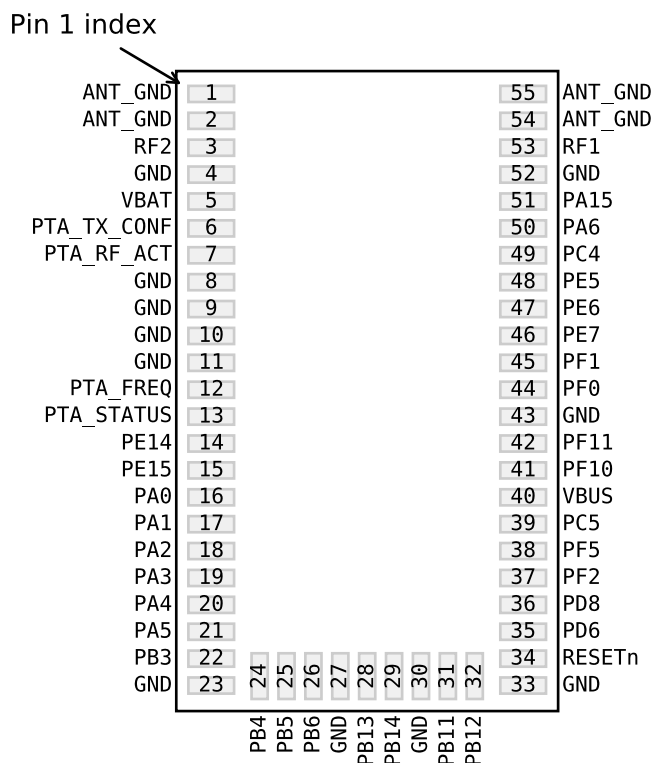


Figure 7.1. WGM160P Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [7.2 GPIO Functionality](#) or [7.3 Alternate Pin Functionality](#).

Table 7.1. WGM160P Device Pinout

| Pin Name | Pin(s)             | Description     | Pin Name | Pin(s) | Description  |
|----------|--------------------|-----------------|----------|--------|--|
| ANT_GND  | 1<br>2<br>54<br>55 | Antenna ground. | RF2      | 3      | External antenna connection for diversity antenna. Terminate to ground with 47-51 Ohms if not connected to an antenna. |



| Pin Name    | Pin(s)  | Description   | Pin Name   | Pin(s) | Description   |
|-------------|---|---|------------|--------|---|
| GND         | 4<br>8<br>9<br>10<br>11<br>23<br>27<br>30<br>33<br>43<br>52 | Ground. Connect all ground pins to ground plane.  | VBAT       | 5      | Module power supply   |
| PTA_TX_CONF | 6   | PTA TX_CONF pin. These pins can be used to manage co-existence with another 2.4 GHz radio.  | PTA_RF_ACT | 7      | PTA RF_ACT pin. These pins can be used to manage co-existence with another 2.4 GHz radio. |
| PTA_FREQ    | 12  | PTA FREQ pin. These pins can be used to manage co-existence with another 2.4 GHz radio.   | PTA_STATUS | 13     | PTA STATUS pin. These pins can be used to manage co-existence with another 2.4 GHz radio. |
| PE14        | 14  | GPIO  | PE15       | 15     | GPIO  |
| PA0         | 16  | GPIO  | PA1        | 17     | GPIO  |
| PA2         | 18  | GPIO  | PA3        | 19     | GPIO  |
| PA4         | 20  | GPIO  | PA5        | 21     | GPIO  |
| PB3         | 22  | GPIO  | PB4        | 24     | GPIO  |
| PB5         | 25  | GPIO  | PB6        | 26     | GPIO  |
| PB13        | 28  | GPIO  | PB14       | 29     | GPIO  |
| PB11        | 31  | GPIO  | PB12       | 32     | GPIO  |
| RESETn      | 34  | Reset input, active low. This pin is internally pulled up to VBAT. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | PD6        | 35     | GPIO  |
| PD8         | 36  | GPIO  | PF2        | 37     | GPIO  |
| PF5         | 38  | GPIO  | PC5        | 39     | GPIO  |
| VBUS        | 40  | USB VBUS signal and auxiliary input to 5 V regulator. May be left disconnected if USB is unused.  | PF10       | 41     | GPIO (5V)   |
| PF11        | 42  | GPIO (5V)   | PF0        | 44     | GPIO (5V)   |
| PF1         | 45  | GPIO (5V)   | PE7        | 46     | GPIO  |
| PE6         | 47  | GPIO  | PE5        | 48     | GPIO  |
| PC4         | 49  | GPIO  | PA6        | 50     | GPIO  |
| PA15        | 51  | GPIO  | RF1        | 53     | External antenna connection on WGM160P22N. Not connected on WGM160P22A.                   |

**Note:**

1. GPIO with 5V tolerance are indicated by (5V).

## 7.2 GPIO Functionality

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of each GPIO pin, followed by the functionality available on that pin. Refer to [7.3 Alternate Pin Functionality](#) for a list of GPIO locations available for each function.

Full peripheral features and flexibility are not supported with all software architectures. Refer to “UG384 WGM160P Hardware Design Users Guide” for more details.

**Table 7.2. GPIO Functionality Table**

| GPIO Name | Pin Alternate Functionality / Description |  |  |  |
|-----------|---|--|--|--|
|           | Analog                                    | Timers   | Communication  | Other  |
| PA0       | BUSBY<br>BUSAX<br>LCD_SEG13               | TIM0_CC0 #0<br>TIM0_CC1 #7<br>TIM3_CC0 #4<br>PCNT0_S0IN #4 | ETH_RMIITXEN<br>US1_RX #5<br>US3_TX #0<br>QSPIO_CS0<br>LEU0_RX #4<br>I2C0_SDA #0 | CMU_CLK2 #0<br>PRS_CH0 #0<br>PRS_CH3<br>GPIO_EM4WU0                            |
| PA1       | BUSAY<br>BUSBX<br>LCD_SEG14               | TIM0_CC0 #7<br>TIM0_CC1 #0<br>TIM3_CC1 #4<br>PCNT0_S1IN #4 | ETH_RMIIRXD1<br>US3_RX #0<br>QSPIO_CS1<br>I2C0_SCL #0                            | CMU_CLK1 #0<br>PRS_CH1   |
| PA2       | BUSBY<br>BUSAX<br>LCD_SEG15               | TIM0_CC2 #0<br>TIM3_CC2 #4                                 | ETH_RMIIRXD0<br>US1_RX #6<br>US3_CLK<br>QSPIO_DQ0                                | CMU_CLK0 #0<br>PRS_CH8<br>ETM_TD0 #3   |
| PA3       | BUSAY<br>BUSBX<br>LCD_SEG16               | TIM0_CDTI0<br>TIM3_CC0 #5                                  | ETH_RMIIREFCLK<br>US3_CS<br>U0_TX #2<br>QSPIO_DQ1                                | CMU_CLK2 #1<br>CMU_CLKI0 #1<br>CMU_CLK2 #4<br>LES_ALTEX2<br>PRS_CH9<br>ETM_TD1 |
| PA4       | BUSBY<br>BUSAX<br>LCD_SEG17               | TIM0_CDTI1<br>TIM3_CC1 #5                                  | ETH_RMIICRSVDV<br>US3_CTS #0<br>U0_RX #2<br>QSPIO_DQ2                            | LES_ALTEX3<br>PRS_CH16 #0<br>ETM_TD2 #3  |
| PA5       | BUSAY<br>BUSBX<br>LCD_SEG18               | TIM0_CDTI2 #0<br>TIM3_CC2 #5<br>PCNT1_S0IN #0              | ETH_RMIIRXER<br>US3_RTS<br>U0_CTS<br>QSPIO_DQ3<br>LEU1_TX #1                     | LES_ALTEX4<br>PRS_CH17 #0<br>ACMP1_O #7<br>ETM_TD3 #3                          |

| GPIO Name | Pin Alternate Functionality / Description               |  |  |   |
|-----------|---|--|--|---|
|           | Analog  | Timers   | Communication  | Other   |
| PA6       | BUSBY<br>BUSAX<br>LCD_SEG19                             | TIM3_CC0 #6<br>WTIM0_CC0 #1<br>LETIM1_OUT1 #0<br>PCNT1_S1IN #0                             | ETH_MDC #3<br>U0_RTS #2<br>LEU1_RX #1                                | PRS_CH6 #0<br>ACMP0_O #4<br>ETM_TCLK<br>GPIO_EM4WU1                     |
| PA15      | BUSAY<br>BUSBX<br>LCD_SEG12                             | TIM3_CC2 #0  | ETH_MDIO #3<br>US2_CLK #3  | PRS_CH15 #0   |
| PB3       | BUSAY<br>BUSBX<br>LCD_SEG20 /<br>LCD_COM4               | TIM1_CC3 #2<br>WTIM0_CC0 #6<br>PCNT1_S0IN #1   | ETH_MDIO #0<br>US2_TX #1<br>US3_TX #2<br>QSPI0_DQ4                   | PRS_CH19 #0<br>ACMP0_O #7   |
| PB4       | BUSBY<br>BUSAX<br>LCD_SEG21 /<br>LCD_COM5               | WTIM0_CC1 #6<br>PCNT1_S1IN #1  | ETH_MDC #0<br>US2_RX #1<br>QSPI0_DQ5<br>LEU1_TX #4                   | PRS_CH20  |
| PB5       | BUSAY<br>BUSBX<br>LCD_SEG22 /<br>LCD_COM6               | WTIM0_CC2 #6<br>LETIM1_OUT0<br>PCNT0_S0IN #6   | ETH_TSUEXTCLK<br>US0_RTS #4<br>US2_CLK #1<br>QSPI0_DQ6<br>LEU1_RX #4 | PRS_CH21 #0   |
| PB6       | BUSBY<br>BUSAX<br>LCD_SEG23 /<br>LCD_COM7               | TIM0_CC0 #3<br>TIM2_CC0 #4<br>WTIM3_CC0<br>LETIM1_OUT1 #4<br>PCNT0_S1IN #6                 | ETH_TSUTMRTOG<br>US0_CTS #4<br>US2_CS #1<br>QSPI0_DQ7                | PRS_CH12 #1   |
| PB11      | BUSAY<br>BUSBX<br>VDAC0_OUT0 /<br>OPA0_OUT<br>IDAC0_OUT | TIM0_CDTI2 #4<br>TIM1_CC2<br>WTIM2_CC2<br>LETIM0_OUT0 #1<br>PCNT0_S1IN #7<br>PCNT1_S0IN #6 | US0_CTS #5<br>US1_CLK #5<br>US2_CS #3<br>U1_CTS #2<br>I2C1_SDA #1    | CMU_CLK1 #5<br>CMU_CLKI0 #7<br>PRS_CH21 #2<br>ACMP0_O #3<br>GPIO_EM4WU7 |
| PB12      | BUSBY<br>BUSAX<br>VDAC0_OUT1 /<br>OPA1_OUT              | TIM1_CC3 #3<br>WTIM2_CC0<br>LETIM0_OUT1 #1<br>PCNT0_S0IN #7<br>PCNT1_S1IN #6               | US2_CTS #1<br>U1_RTS #2<br>I2C1_SCL #1                               | PRS_CH16 #1   |

| GPIO Name | Pin Alternate Functionality / Description                             |   |   |  |
|-----------|---|---|---|--|
|           | Analog  | Timers  | Communication   | Other  |
| PB13      | BUSAY<br>BUSBX<br>HFXTAL_P  | TIM6_CC0<br>WTIM1_CC0 #0<br>PCNT2_S0IN #2   | US0_CLK #4<br>US1_CTS<br>LEU0_TX #1   | CMU_CLKI0 #3<br>PRS_CH7 #0                                       |
| PB14      | BUSBY<br>BUSAX<br>HFXTAL_N  | TIM6_CC1<br>WTIM1_CC1<br>PCNT2_S1IN #2  | US0_CS<br>US1_RTS<br>LEU0_RX #1   | PRS_CH6 #1   |
| PC4       | BUSACMP0Y<br>BUSACMP0X<br>OPA0_P                                      | TIM0_CC0 #5<br>TIM0_CDTI2 #3<br>TIM2_CC2<br>LETIM0_OUT0 #3<br>PCNT1_S0IN #3               | US2_CLK #0<br>U0_TX #4<br>U1_CTS #4<br>I2C1_SDA #0                              | LES_CH4<br>PRS_CH18<br>GPIO_EM4WU6                               |
| PC5       | BUSACMP0Y<br>BUSACMP0X<br>OPA0_N                                      | TIM0_CC1 #5<br>LETIM0_OUT1 #3<br>PCNT1_S1IN #3  | US2_CS #0<br>U0_RX #4<br>U1_RTS #4<br>I2C1_SCL #0                               | LES_CH5<br>PRS_CH19 #2   |
| PD6       | BUSADC0Y<br>BUSADC0X<br>ADC0_EXTP<br>VDAC0_EXT<br>ADC1_EXTP<br>OPA1_P | TIM1_CC0 #4<br>TIM6_CC2<br>WTIM0_CDTI2<br>WTIM1_CC0 #2<br>LETIM0_OUT0 #0<br>PCNT0_S0IN #3 | US0_RTS #5<br>US1_RX #2<br>US2_CTS #5<br>US3_CTS #2<br>U0_RTS #5<br>I2C0_SDA #1 | CMU_CLK2 #2<br>LES_ALTEX0<br>PRS_CH5<br>ACMP0_O #2<br>ETM_TD0 #0 |
| PD8       | BU_VIN  | WTIM1_CC2 #2  | US2_RTS   | CMU_CLK1 #1<br>PRS_CH12 #2<br>ACMP2_O                            |
| PE5       | BUSCY<br>BUSDX<br>LCD_COM1  | TIM3_CC0 #3<br>TIM3_CC2 #2<br>TIM5_CC1 #0<br>TIM6_CDTI1<br>WTIM0_CC1 #0<br>WTIM1_CC2 #4   | US0_CLK #1<br>US1_CLK #6<br>US3_CTS #1<br>U1_RTS #3<br>I2C0_SCL #7              | PRS_CH17 #2  |
| PE6       | BUSDY<br>BUSCX<br>LCD_COM2  | TIM3_CC1 #3<br>TIM5_CC2 #0<br>TIM6_CDTI2<br>WTIM0_CC2 #0<br>WTIM1_CC3                     | US0_RX<br>US3_TX #1   | PRS_CH6 #2   |

| GPIO Name | Pin Alternate Functionality / Description |   |  |  |
|-----------|---|---|--|--|
|           | Analog                                    | Timers  | Communication  | Other  |
| PE7       | BUSCY<br>BUSDX<br>LCD_COM3                | TIM3_CC2 #3<br>TIM5_CC0<br>WTIM1_CC0 #5       | US0_TX<br>US3_RX #1  | PRS_CH7 #2   |
| PE14      | BUSDY<br>BUSCX<br>LCD_SEG10               | TIM2_CDTI1<br>TIM3_CC0 #0                     | ETH_RMIITXD1<br>US0_CTS #0<br>QSPIO_SCLK<br>LEU0_TX #2                   | PRS_CH13<br>ETM_TD2 #4   |
| PE15      | BUSCY<br>BUSDX<br>LCD_SEG11               | TIM2_CDTI2<br>TIM3_CC1 #0                     | ETH_RMIITXD0<br>US0_RTS #0<br>QSPIO_DQS<br>LEU0_RX #2                    | PRS_CH14<br>ETM_TD3 #4   |
| PF0       | BUSDY<br>BUSCX                            | TIM0_CC0 #4<br>WTIM0_CC1 #4<br>LETIM0_OUT0 #2 | US2_TX #5<br>CAN0_RX<br>US1_CLK #2<br>LEU0_TX #3<br>I2C0_SDA #5          | PRS_CH15 #2<br>ACMP3_O<br>DBG_SWCLKTCK<br>BOOT_TX                            |
| PF1       | BUSCY<br>BUSDX                            | TIM0_CC1 #4<br>WTIM0_CC2 #4<br>LETIM0_OUT1 #2 | US2_RX #5<br>US1_CS<br>U0_TX #5<br>LEU0_RX #3<br>I2C0_SCL #5             | PRS_CH4<br>DBG_SWDIOTMS<br>GPIO_EM4WU3<br>BOOT_RX                            |
| PF2       | BUSDY<br>BUSCX<br>LCD_SEG0                | TIM0_CC2 #4<br>TIM1_CC0 #5<br>TIM2_CC0 #3     | US2_CLK #5<br>CAN0_TX<br>US1_TX<br>U0_RX #5<br>LEU0_TX #4<br>I2C1_SCL #4 | CMU_CLK0 #4<br>PRS_CH0 #3<br>ACMP1_O #0<br>DBG_TDO<br>DBG_SWO<br>GPIO_EM4WU4 |
| PF5       | BUSCY<br>BUSDX<br>LCD_SEG3                | TIM0_CDTI2 #2<br>TIM1_CC3 #6<br>TIM4_CC0      | US2_CS #5<br>I2C2_SCL #0<br>USB_VBUSEN                                   | PRS_CH2<br>DBG_TDI   |
| PF10      | BUSDY<br>BUSCX                            | TIM5_CC1 #6<br>WTIM3_CC1<br>PCNT2_S0IN #3     | U1_TX<br>I2C2_SDA<br>USB_DM  |  |
| PF11      | BUSCY<br>BUSDX                            | TIM5_CC2 #6<br>WTIM3_CC2<br>PCNT2_S1IN #3     | U1_RX<br>I2C2_SCL #2<br>USB_DP   |  |

### 7.3 Alternate Pin Functionality

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings and the associated GPIO pin. Refer to [7.2 GPIO Functionality](#) for a list of functions available on each GPIO pin.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 7.3. Alternate Functionality Overview**

| Alternate<br>Functionality | LOCATION                   |                  | Description   |
|----------------------------|----------------------------|------------------|---|
|                            | 0 - 3                      | 4 - 7            |   |
| ACMP0_O                    | 2: PD6<br>3: PB11          | 4: PA6<br>7: PB3 | Analog comparator ACMP0, digital output.  |
| ACMP1_O                    | 0: PF2                     | 7: PA5           | Analog comparator ACMP1, digital output.  |
| ACMP2_O                    | 0: PD8                     |                  | Analog comparator ACMP2, digital output.  |
| ACMP3_O                    | 0: PF0                     |                  | Analog comparator ACMP3, digital output.  |
| ADC0_EXTP                  | 0: PD6                     |                  | Analog to digital converter ADC0 external reference input positive pin.   |
| ADC1_EXTP                  | 0: PD6                     |                  | Analog to digital converter ADC1 external reference input positive pin.   |
| BOOT_RX                    | 0: PF1                     |                  | Bootloader RX.  |
| BOOT_TX                    | 0: PF0                     |                  | Bootloader TX.  |
| BU_VIN                     | 0: PD8                     |                  | Battery input for Backup Power Domain.  |
| CAN0_RX                    | 1: PF0                     |                  | CAN0 RX.  |
| CAN0_TX                    | 1: PF2                     |                  | CAN0 TX.  |
| CMU_CLK0                   | 0: PA2                     | 4: PF2           | Clock Management Unit, clock output number 0.   |
| CMU_CLK1                   | 0: PA1<br>1: PD8           | 5: PB11          | Clock Management Unit, clock output number 1.   |
| CMU_CLK2                   | 0: PA0<br>1: PA3<br>2: PD6 | 4: PA3           | Clock Management Unit, clock output number 2.   |
| CMU_CLKI0                  | 1: PA3<br>3: PB13          | 7: PB11          | Clock Management Unit, clock input number 0.  |
| DBG_SWCLKTCK               | 0: PF0                     |                  | Debug-interface Serial Wire clock input and JTAG Test Clock.<br>Note that this function is enabled to the pin out of reset, and has a built-in pull down.             |
| DBG_SWDIOTMS               | 0: PF1                     |                  | Debug-interface Serial Wire data input / output and JTAG Test Mode Select.<br>Note that this function is enabled to the pin out of reset, and has a built-in pull up. |
| DBG_SWO                    | 0: PF2                     |                  | Debug-interface Serial Wire viewer Output.<br>Note that this function is not enabled after reset, and must be enabled by software to be used.                         |

| Alternate        | LOCATION          |                  | Description   |
|------------------|-------------------|------------------|---|
|                  | 0 - 3             | 4 - 7            |   |
| DBG_TDI          | 0: PF5            |                  | Debug-interface JTAG Test Data In.<br><br>Note that this function becomes available after the first valid JTAG command is received, and has a built-in pull up when JTAG is active. |
| DBG_TDO          | 0: PF2            |                  | Debug-interface JTAG Test Data Out.<br><br>Note that this function becomes available after the first valid JTAG command is received.  |
| ETH_MDC          | 0: PB4<br>3: PA6  |                  | Ethernet Management Data Clock.   |
| ETH_MDIO         | 0: PB3<br>3: PA15 |                  | Ethernet Management Data I/O.   |
| ETH_RMII CRS DV  | 0: PA4            |                  | Ethernet RMII Carrier Sense / Data Valid.   |
| ETH_RMII REF CLK | 0: PA3            |                  | Ethernet RMII Reference Clock.  |
| ETH_RMII RX D0   | 0: PA2            |                  | Ethernet RMII Receive Data Bit 0.   |
| ETH_RMII RX D1   | 0: PA1            |                  | Ethernet RMII Receive Data Bit 1.   |
| ETH_RMII RX ER   | 0: PA5            |                  | Ethernet RMII Receive Error.  |
| ETH_RMII TX D0   | 0: PE15           |                  | Ethernet RMII Transmit Data Bit 0.  |
| ETH_RMII TX D1   | 0: PE14           |                  | Ethernet RMII Transmit Data Bit 1.  |
| ETH_RMII TX EN   | 0: PA0            |                  | Ethernet RMII Transmit Enable.  |
| ETH_TSU EXT CLK  | 0: PB5            |                  | Ethernet IEEE1588 External Reference Clock.   |
| ETH_TSU TMR-TOG  | 0: PB6            |                  | Ethernet IEEE1588 Timer Toggle.   |
| ETM_TCLK         | 3: PA6            |                  | Embedded Trace Module ETM clock .   |
| ETM_TD0          | 0: PD6<br>3: PA2  |                  | Embedded Trace Module ETM data 0.   |
| ETM_TD1          | 3: PA3            |                  | Embedded Trace Module ETM data 1.   |
| ETM_TD2          | 3: PA4            | 4: PE14          | Embedded Trace Module ETM data 2.   |
| ETM_TD3          | 3: PA5            | 4: PE15          | Embedded Trace Module ETM data 3.   |
| GPIO_EM4WU0      | 0: PA0            |                  | Pin can be used to wake the system up from EM4  |
| GPIO_EM4WU1      | 0: PA6            |                  | Pin can be used to wake the system up from EM4  |
| GPIO_EM4WU3      | 0: PF1            |                  | Pin can be used to wake the system up from EM4  |
| GPIO_EM4WU4      | 0: PF2            |                  | Pin can be used to wake the system up from EM4  |
| GPIO_EM4WU6      | 0: PC4            |                  | Pin can be used to wake the system up from EM4  |
| GPIO_EM4WU7      | 0: PB11           |                  | Pin can be used to wake the system up from EM4  |
| HFX TAL_N        | 0: PB14           |                  | High Frequency Crystal negative pin. Also used as external optional clock input pin.  |
| HFX TAL_P        | 0: PB13           |                  | High Frequency Crystal positive pin.  |
| I2C0_SCL         | 0: PA1            | 5: PF1<br>7: PE5 | I2C0 Serial Clock Line input / output.  |

| Alternate               | LOCATION          |        | Description  |
|-------------------------|-------------------|--------|--|
|                         | 0 - 3             | 4 - 7  |  |
| I2C0_SDA                | 0: PA0<br>1: PD6  | 5: PF0 | I2C0 Serial Data input / output.                                 |
| I2C1_SCL                | 0: PC5<br>1: PB12 | 4: PF2 | I2C1 Serial Clock Line input / output.                           |
| I2C1_SDA                | 0: PC4<br>1: PB11 |        | I2C1 Serial Data input / output.                                 |
| I2C2_SCL                | 0: PF5<br>2: PF11 |        | I2C2 Serial Clock Line input / output.                           |
| I2C2_SDA                | 2: PF10           |        | I2C2 Serial Data input / output.                                 |
| IDAC0_OUT               | 0: PB11           |        | IDAC0 output.  |
| LCD_COM1                | 0: PE5            |        | LCD driver common line number 1.                                 |
| LCD_COM2                | 0: PE6            |        | LCD driver common line number 2.                                 |
| LCD_COM3                | 0: PE7            |        | LCD driver common line number 3.                                 |
| LCD_SEG0                | 0: PF2            |        | LCD segment line 0.  |
| LCD_SEG3                | 0: PF5            |        | LCD segment line 3.  |
| LCD_SEG10               | 0: PE14           |        | LCD segment line 10.   |
| LCD_SEG11               | 0: PE15           |        | LCD segment line 11.   |
| LCD_SEG12               | 0: PA15           |        | LCD segment line 12.   |
| LCD_SEG13               | 0: PA0            |        | LCD segment line 13.   |
| LCD_SEG14               | 0: PA1            |        | LCD segment line 14.   |
| LCD_SEG15               | 0: PA2            |        | LCD segment line 15.   |
| LCD_SEG16               | 0: PA3            |        | LCD segment line 16.   |
| LCD_SEG17               | 0: PA4            |        | LCD segment line 17.   |
| LCD_SEG18               | 0: PA5            |        | LCD segment line 18.   |
| LCD_SEG19               | 0: PA6            |        | LCD segment line 19.   |
| LCD_SEG20 /<br>LCD_COM4 | 0: PB3            |        | LCD segment line 20. This pin may also be used as LCD COM line 4 |
| LCD_SEG21 /<br>LCD_COM5 | 0: PB4            |        | LCD segment line 21. This pin may also be used as LCD COM line 5 |
| LCD_SEG22 /<br>LCD_COM6 | 0: PB5            |        | LCD segment line 22. This pin may also be used as LCD COM line 6 |
| LCD_SEG23 /<br>LCD_COM7 | 0: PB6            |        | LCD segment line 23. This pin may also be used as LCD COM line 7 |
| LES_ALTEX0              | 0: PD6            |        | LESENSE alternate excite output 0.                               |
| LES_ALTEX2              | 0: PA3            |        | LESENSE alternate excite output 2.                               |
| LES_ALTEX3              | 0: PA4            |        | LESENSE alternate excite output 3.                               |
| LES_ALTEX4              | 0: PA5            |        | LESENSE alternate excite output 4.                               |
| LES_CH4                 | 0: PC4            |        | LESENSE channel 4.   |



| Alternate   | LOCATION                              |                             | Description   |
|-------------|---------------------------------------|-----------------------------|---|
|             | 0 - 3                                 | 4 - 7                       |   |
| LES_CH5     | 0: PC5                                |                             | LESENSE channel 5.  |
| LETIM0_OUT0 | 0: PD6<br>1: PB11<br>2: PF0<br>3: PC4 |                             | Low Energy Timer LETIM0, output channel 0.  |
| LETIM0_OUT1 | 1: PB12<br>2: PF1<br>3: PC5           |                             | Low Energy Timer LETIM0, output channel 1.  |
| LETIM1_OUT0 |                                       | 4: PB5                      | Low Energy Timer LETIM1, output channel 0.  |
| LETIM1_OUT1 | 0: PA6                                | 4: PB6                      | Low Energy Timer LETIM1, output channel 1.  |
| LEU0_RX     | 1: PB14<br>2: PE15<br>3: PF1          | 4: PA0                      | LEUART0 Receive input.  |
| LEU0_TX     | 1: PB13<br>2: PE14<br>3: PF0          | 4: PF2                      | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX     | 1: PA6                                | 4: PB5                      | LEUART1 Receive input.  |
| LEU1_TX     | 1: PA5                                | 4: PB4                      | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| OPA0_N      | 0: PC5                                |                             | Operational Amplifier 0 external negative input.                                  |
| OPA0_P      | 0: PC4                                |                             | Operational Amplifier 0 external positive input.                                  |
| OPA1_P      | 0: PD6                                |                             | Operational Amplifier 1 external positive input.                                  |
| PCNT0_S0IN  | 3: PD6                                | 4: PA0<br>6: PB5<br>7: PB12 | Pulse Counter PCNT0 input number 0.   |
| PCNT0_S1IN  |                                       | 4: PA1<br>6: PB6<br>7: PB11 | Pulse Counter PCNT0 input number 1.   |
| PCNT1_S0IN  | 0: PA5<br>1: PB3<br>3: PC4            | 6: PB11                     | Pulse Counter PCNT1 input number 0.   |
| PCNT1_S1IN  | 0: PA6<br>1: PB4<br>3: PC5            | 6: PB12                     | Pulse Counter PCNT1 input number 1.   |
| PCNT2_S0IN  | 2: PB13<br>3: PF10                    |                             | Pulse Counter PCNT2 input number 0.   |

| Alternate  | LOCATION                    |       | Description                               |
|------------|-----------------------------|-------|---|
|            | 0 - 3                       | 4 - 7 |   |
| PCNT2_S1IN | 2: PB14<br>3: PF11          |       | Pulse Counter PCNT2 input number 1.       |
| PRS_CH0    | 0: PA0<br>3: PF2            |       | Peripheral Reflex System PRS, channel 0.  |
| PRS_CH1    | 0: PA1                      |       | Peripheral Reflex System PRS, channel 1.  |
| PRS_CH2    | 1: PF5                      |       | Peripheral Reflex System PRS, channel 2.  |
| PRS_CH3    | 3: PA0                      |       | Peripheral Reflex System PRS, channel 3.  |
| PRS_CH4    | 2: PF1                      |       | Peripheral Reflex System PRS, channel 4.  |
| PRS_CH5    | 2: PD6                      |       | Peripheral Reflex System PRS, channel 5.  |
| PRS_CH6    | 0: PA6<br>1: PB14<br>2: PE6 |       | Peripheral Reflex System PRS, channel 6.  |
| PRS_CH7    | 0: PB13<br>2: PE7           |       | Peripheral Reflex System PRS, channel 7.  |
| PRS_CH8    | 1: PA2                      |       | Peripheral Reflex System PRS, channel 8.  |
| PRS_CH9    | 1: PA3                      |       | Peripheral Reflex System PRS, channel 9.  |
| PRS_CH12   | 1: PB6<br>2: PD8            |       | Peripheral Reflex System PRS, channel 12. |
| PRS_CH13   | 2: PE14                     |       | Peripheral Reflex System PRS, channel 13. |
| PRS_CH14   | 2: PE15                     |       | Peripheral Reflex System PRS, channel 14. |
| PRS_CH15   | 0: PA15<br>2: PF0           |       | Peripheral Reflex System PRS, channel 15. |
| PRS_CH16   | 0: PA4<br>1: PB12           |       | Peripheral Reflex System PRS, channel 16. |
| PRS_CH17   | 0: PA5<br>2: PE5            |       | Peripheral Reflex System PRS, channel 17. |
| PRS_CH18   | 2: PC4                      |       | Peripheral Reflex System PRS, channel 18. |
| PRS_CH19   | 0: PB3<br>2: PC5            |       | Peripheral Reflex System PRS, channel 19. |
| PRS_CH20   | 0: PB4                      |       | Peripheral Reflex System PRS, channel 20. |
| PRS_CH21   | 0: PB5<br>2: PB11           |       | Peripheral Reflex System PRS, channel 21. |
| QSPI0_CS0  | 1: PA0                      |       | Quad SPI 0 Chip Select 0.                 |
| QSPI0_CS1  | 1: PA1                      |       | Quad SPI 0 Chip Select 1.                 |
| QSPI0_DQ0  | 1: PA2                      |       | Quad SPI 0 Data 0.                        |
| QSPI0_DQ1  | 1: PA3                      |       | Quad SPI 0 Data 1.                        |

| Alternate  | LOCATION                   |                            | Description  |
|------------|----------------------------|----------------------------|--|
|            | 0 - 3                      | 4 - 7                      |  |
| QSPI0_DQ2  | 1: PA4                     |                            | Quad SPI 0 Data 2.                                   |
| QSPI0_DQ3  | 1: PA5                     |                            | Quad SPI 0 Data 3.                                   |
| QSPI0_DQ4  | 1: PB3                     |                            | Quad SPI 0 Data 4.                                   |
| QSPI0_DQ5  | 1: PB4                     |                            | Quad SPI 0 Data 5.                                   |
| QSPI0_DQ6  | 1: PB5                     |                            | Quad SPI 0 Data 6.                                   |
| QSPI0_DQ7  | 1: PB6                     |                            | Quad SPI 0 Data 7.                                   |
| QSPI0_DQS  | 1: PE15                    |                            | Quad SPI 0 Data S.                                   |
| QSPI0_SCLK | 1: PE14                    |                            | Quad SPI 0 Serial Clock.                             |
| TIM0_CC0   | 0: PA0<br>3: PB6           | 4: PF0<br>5: PC4<br>7: PA1 | Timer 0 Capture Compare input / output channel 0.    |
| TIM0_CC1   | 0: PA1                     | 4: PF1<br>5: PC5<br>7: PA0 | Timer 0 Capture Compare input / output channel 1.    |
| TIM0_CC2   | 0: PA2                     | 4: PF2                     | Timer 0 Capture Compare input / output channel 2.    |
| TIM0_CDT10 | 0: PA3                     |                            | Timer 0 Complimentary Dead Time Insertion channel 0. |
| TIM0_CDT11 | 0: PA4                     |                            | Timer 0 Complimentary Dead Time Insertion channel 1. |
| TIM0_CDT12 | 0: PA5<br>2: PF5<br>3: PC4 | 4: PB11                    | Timer 0 Complimentary Dead Time Insertion channel 2. |
| TIM1_CC0   |                            | 4: PD6<br>5: PF2           | Timer 1 Capture Compare input / output channel 0.    |
| TIM1_CC2   | 3: PB11                    |                            | Timer 1 Capture Compare input / output channel 2.    |
| TIM1_CC3   | 2: PB3<br>3: PB12          | 6: PF5                     | Timer 1 Capture Compare input / output channel 3.    |
| TIM2_CC0   | 3: PF2                     | 4: PB6                     | Timer 2 Capture Compare input / output channel 0.    |
| TIM2_CC2   |                            | 5: PC4                     | Timer 2 Capture Compare input / output channel 2.    |
| TIM2_CDT11 | 2: PE14                    |                            | Timer 2 Complimentary Dead Time Insertion channel 1. |
| TIM2_CDT12 | 2: PE15                    |                            | Timer 2 Complimentary Dead Time Insertion channel 2. |
| TIM3_CC0   | 0: PE14<br>3: PE5          | 4: PA0<br>5: PA3<br>6: PA6 | Timer 3 Capture Compare input / output channel 0.    |
| TIM3_CC1   | 0: PE15<br>3: PE6          | 4: PA1<br>5: PA4           | Timer 3 Capture Compare input / output channel 1.    |

| Alternate  | LOCATION                    |                   | Description   |
|------------|-----------------------------|-------------------|---|
|            | 0 - 3                       | 4 - 7             |   |
| TIM3_CC2   | 0: PA15<br>2: PE5<br>3: PE7 | 4: PA2<br>5: PA5  | Timer 3 Capture Compare input / output channel 2.   |
| TIM4_CC0   | 2: PF5                      |                   | Timer 4 Capture Compare input / output channel 0.   |
| TIM5_CC0   | 1: PE7                      |                   | Timer 5 Capture Compare input / output channel 0.   |
| TIM5_CC1   | 0: PE5                      | 6: PF10           | Timer 5 Capture Compare input / output channel 1.   |
| TIM5_CC2   | 0: PE6                      | 6: PF11           | Timer 5 Capture Compare input / output channel 2.   |
| TIM6_CC0   |                             | 5: PB13           | Timer 6 Capture Compare input / output channel 0.   |
| TIM6_CC1   |                             | 5: PB14           | Timer 6 Capture Compare input / output channel 1.   |
| TIM6_CC2   |                             | 7: PD6            | Timer 6 Capture Compare input / output channel 2.   |
| TIM6_CDT11 | 2: PE5                      |                   | Timer 6 Complimentary Dead Time Insertion channel 1.  |
| TIM6_CDT12 | 2: PE6                      |                   | Timer 6 Complimentary Dead Time Insertion channel 2.  |
| U0_CTS     | 2: PA5                      |                   | UART0 Clear To Send hardware flow control input.  |
| U0_RTS     | 2: PA6                      | 5: PD6            | UART0 Request To Send hardware flow control output.   |
| U0_RX      | 2: PA4                      | 4: PC5<br>5: PF2  | UART0 Receive input.  |
| U0_TX      | 2: PA3                      | 4: PC4<br>5: PF1  | UART0 Transmit output. Also used as receive input in half duplex communication.   |
| U1_CTS     | 2: PB11                     | 4: PC4            | UART1 Clear To Send hardware flow control input.  |
| U1_RTS     | 2: PB12<br>3: PE5           | 4: PC5            | UART1 Request To Send hardware flow control output.   |
| U1_RX      | 1: PF11                     |                   | UART1 Receive input.  |
| U1_TX      | 1: PF10                     |                   | UART1 Transmit output. Also used as receive input in half duplex communication.   |
| US0_CLK    | 1: PE5                      | 4: PB13           | USART0 clock input / output.  |
| US0_CS     |                             | 4: PB14           | USART0 chip select input / output.  |
| US0_CTS    | 0: PE14                     | 4: PB6<br>5: PB11 | USART0 Clear To Send hardware flow control input.   |
| US0_RTS    | 0: PE15                     | 4: PB5<br>5: PD6  | USART0 Request To Send hardware flow control output.  |
| US0_RX     | 1: PE6                      |                   | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO).   |
| US0_TX     | 1: PE7                      |                   | USART0 Asynchronous Transmit. Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK    | 2: PF0                      | 5: PB11<br>6: PE5 | USART1 clock input / output.  |

| Alternate  | LOCATION                    |                  | Description   |
|------------|-----------------------------|------------------|---|
|            | 0 - 3                       | 4 - 7            |   |
| US1_CS     | 2: PF1                      |                  | USART1 chip select input / output.  |
| US1_CTS    |                             | 5: PB13          | USART1 Clear To Send hardware flow control input.   |
| US1_RTS    |                             | 5: PB14          | USART1 Request To Send hardware flow control output.  |
| US1_RX     | 2: PD6                      | 5: PA0<br>6: PA2 | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO).   |
| US1_TX     |                             | 5: PF2           | USART1 Asynchronous Transmit. Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK    | 0: PC4<br>1: PB5<br>3: PA15 | 5: PF2           | USART2 clock input / output.  |
| US2_CS     | 0: PC5<br>1: PB6<br>3: PB11 | 5: PF5           | USART2 chip select input / output.  |
| US2_CTS    | 1: PB12                     | 5: PD6           | USART2 Clear To Send hardware flow control input.   |
| US2_RTS    |                             | 5: PD8           | USART2 Request To Send hardware flow control output.  |
| US2_RX     | 1: PB4                      | 5: PF1           | USART2 Asynchronous Receive.<br>USART2 Synchronous mode Master Input / Slave Output (MISO).   |
| US2_TX     | 1: PB3                      | 5: PF0           | USART2 Asynchronous Transmit. Also used as receive input in half duplex communication.<br>USART2 Synchronous mode Master Output / Slave Input (MOSI). |
| US3_CLK    | 0: PA2                      |                  | USART3 clock input / output.  |
| US3_CS     | 0: PA3                      |                  | USART3 chip select input / output.  |
| US3_CTS    | 0: PA4<br>1: PE5<br>2: PD6  |                  | USART3 Clear To Send hardware flow control input.   |
| US3_RTS    | 0: PA5                      |                  | USART3 Request To Send hardware flow control output.  |
| US3_RX     | 0: PA1<br>1: PE7            |                  | USART3 Asynchronous Receive.<br>USART3 Synchronous mode Master Input / Slave Output (MISO).   |
| US3_TX     | 0: PA0<br>1: PE6<br>2: PB3  |                  | USART3 Asynchronous Transmit. Also used as receive input in half duplex communication.<br>USART3 Synchronous mode Master Output / Slave Input (MOSI). |
| USB_DM     | 0: PF10                     |                  | USB D- pin.   |
| USB_DP     | 0: PF11                     |                  | USB D+ pin.   |
| USB_VBUSEN | 0: PF5                      |                  | USB 5 V VBUS enable.  |
| VDAC0_EXT  | 0: PD6                      |                  | Digital to analog converter VDAC0 external reference input pin.   |

| Alternate             | LOCATION          |                  | Description   |
|-----------------------|-------------------|------------------|---|
|                       | 0 - 3             | 4 - 7            |   |
| VDAC0_OUT0 / OPA0_OUT | 0: PB11           |                  | Digital to Analog Converter DAC0 output channel number 0. |
| VDAC0_OUT1 / OPA1_OUT | 0: PB12           |                  | Digital to Analog Converter DAC0 output channel number 1. |
| WTIM0_CC0             | 1: PA6            | 6: PB3           | Wide timer 0 Capture Compare input / output channel 0.    |
| WTIM0_CC1             | 0: PE5            | 4: PF0<br>6: PB4 | Wide timer 0 Capture Compare input / output channel 1.    |
| WTIM0_CC2             | 0: PE6            | 4: PF1<br>6: PB5 | Wide timer 0 Capture Compare input / output channel 2.    |
| WTIM0_CDTI2           |                   | 4: PD6           | Wide timer 0 Complimentary Dead Time Insertion channel 2. |
| WTIM1_CC0             | 0: PB13<br>2: PD6 | 5: PE7           | Wide timer 1 Capture Compare input / output channel 0.    |
| WTIM1_CC1             | 0: PB14           |                  | Wide timer 1 Capture Compare input / output channel 1.    |
| WTIM1_CC2             | 2: PD8            | 4: PE5           | Wide timer 1 Capture Compare input / output channel 2.    |
| WTIM1_CC3             |                   | 4: PE6           | Wide timer 1 Capture Compare input / output channel 3.    |
| WTIM2_CC0             | 3: PB12           |                  | Wide timer 2 Capture Compare input / output channel 0.    |
| WTIM2_CC2             | 2: PB11           |                  | Wide timer 2 Capture Compare input / output channel 2.    |
| WTIM3_CC0             |                   | 6: PB6           | Wide timer 3 Capture Compare input / output channel 0.    |
| WTIM3_CC1             | 3: PF10           |                  | Wide timer 3 Capture Compare input / output channel 1.    |
| WTIM3_CC2             | 3: PF11           |                  | Wide timer 3 Capture Compare input / output channel 2.    |

Certain alternate function locations may have non-interference priority. These locations will take precedence over any other functions selected on that pin (i.e. another alternate function enabled to the same pin inadvertently).

Some alternate functions may also have high speed priority on certain locations. These locations ensure the fastest possible paths to the pins for timing-critical signals.

The following table lists the alternate functions and locations with special priority.

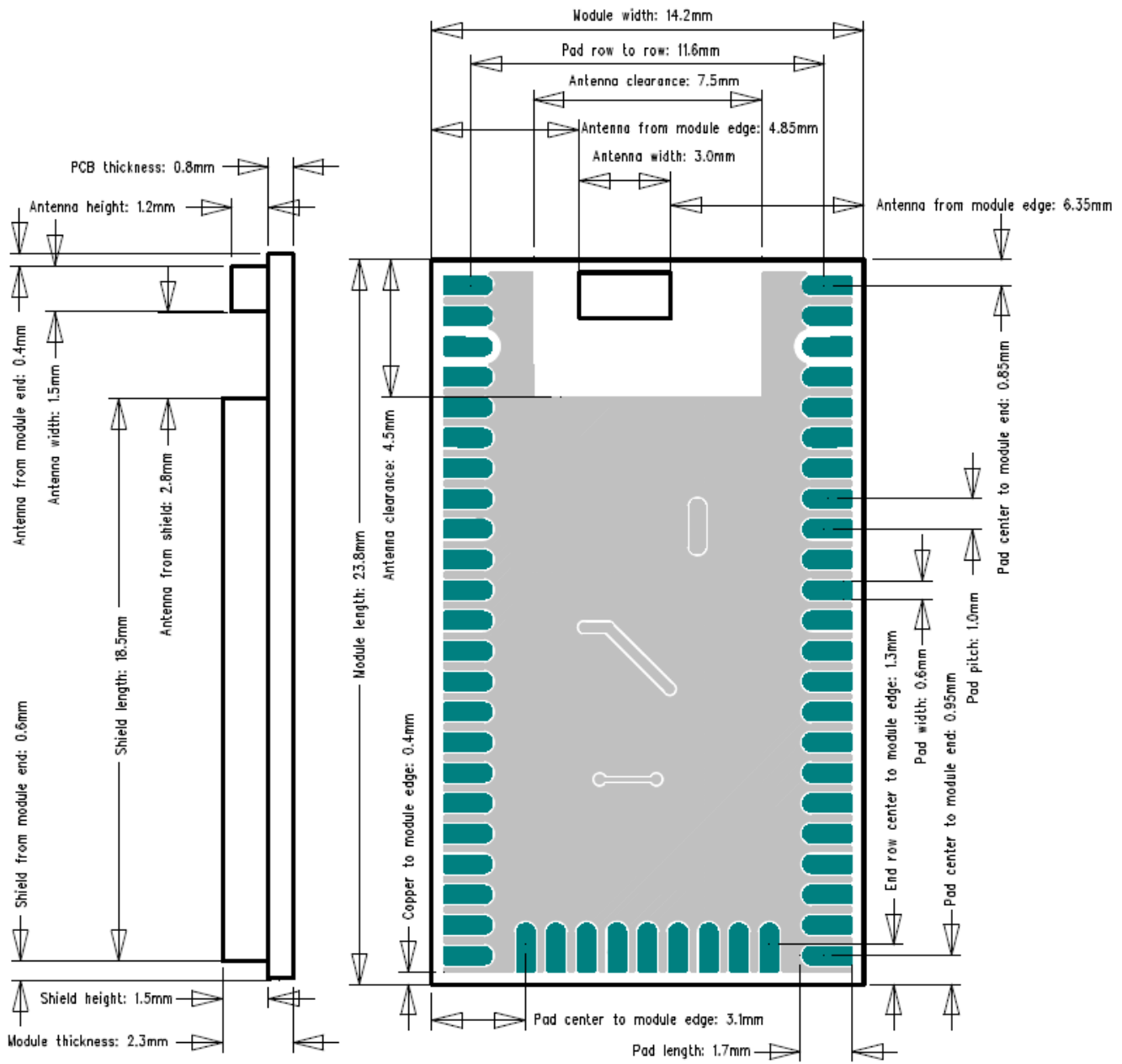
**Table 7.4. Alternate Functionality Priority**

| Alternate Functionality | Location | Priority   |
|-------------------------|----------|------------|
| CMU_CLK2                | 1: PA3   | High Speed |
| CMU_CLKI0               | 1: PA3   | High Speed |
| ETH_RMIICRSVDV          | 0: PA4   | High Speed |
| ETH_RMIIREFCLK          | 0: PA3   | High Speed |
| ETH_RMIIRXD0            | 0: PA2   | High Speed |
| ETH_RMIIRXD1            | 0: PA1   | High Speed |
| ETH_RMIIRXER            | 0: PA5   | High Speed |
| ETH_RMIITXD0            | 0: PE15  | High Speed |
| ETH_RMIITXD1            | 0: PE14  | High Speed |

| Alternate Functionality | Location | Priority         |
|-------------------------|----------|------------------|
| ETH_RMITXEN             | 0: PA0   | High Speed       |
| TIM0_CC0                | 3: PB6   | Non-interference |
| US2_CLK                 | 5: PF2   | High Speed       |
| US2_CS                  | 5: PF5   | High Speed       |
| US2_RX                  | 5: PF1   | High Speed       |
| US2_TX                  | 5: PF0   | High Speed       |

## 8. Package Specifications

### 8.1 Package Outline



**Tolerances  $\pm 0.1\text{mm}$**   
**Module width and length  $\pm 0.2\text{mm}$**

Figure 8.1. WGM160P Package Outline



## 8.2 Recommended PCB Land Patterns

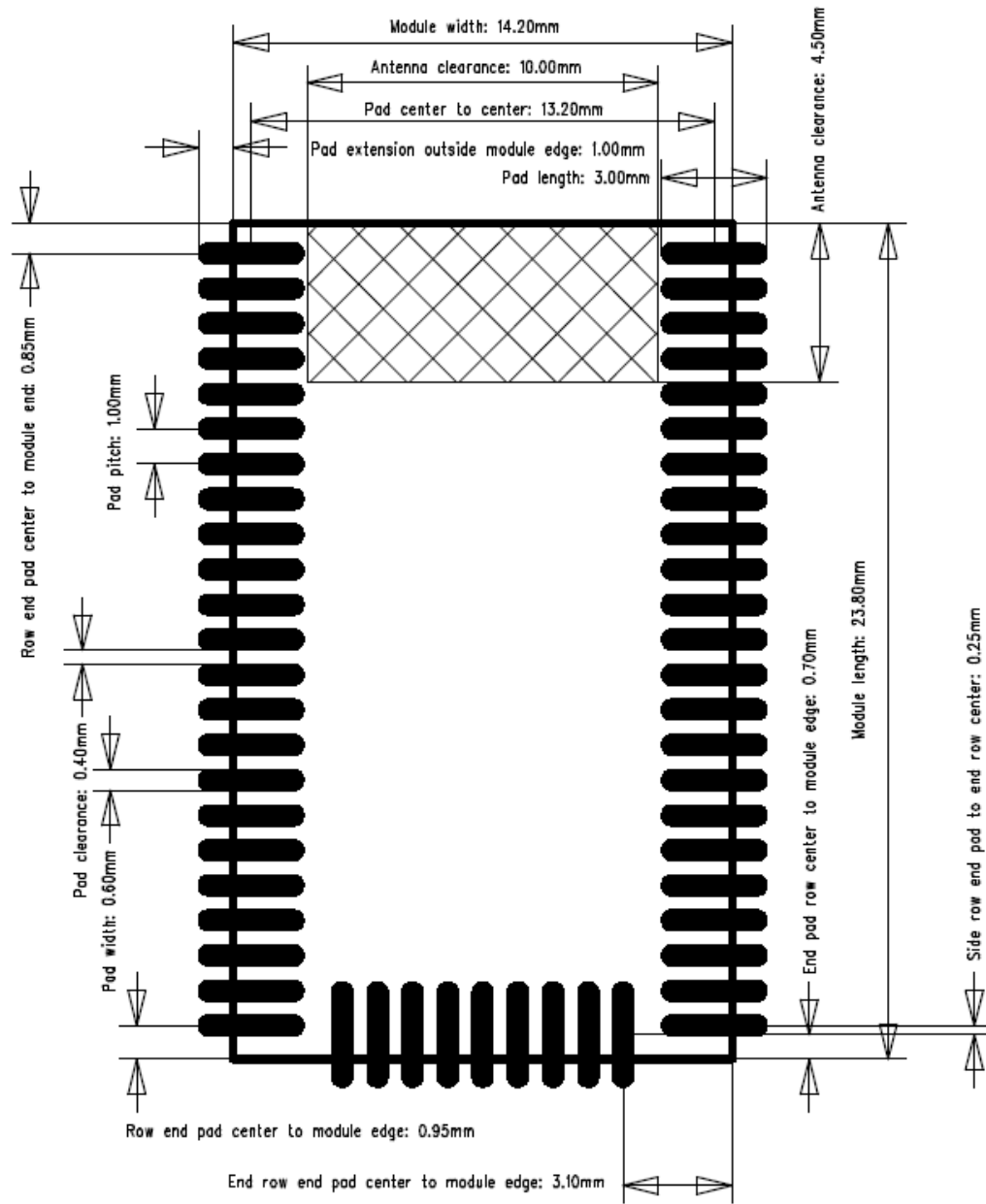


Figure 8.2. WGM160P22A Land Pattern

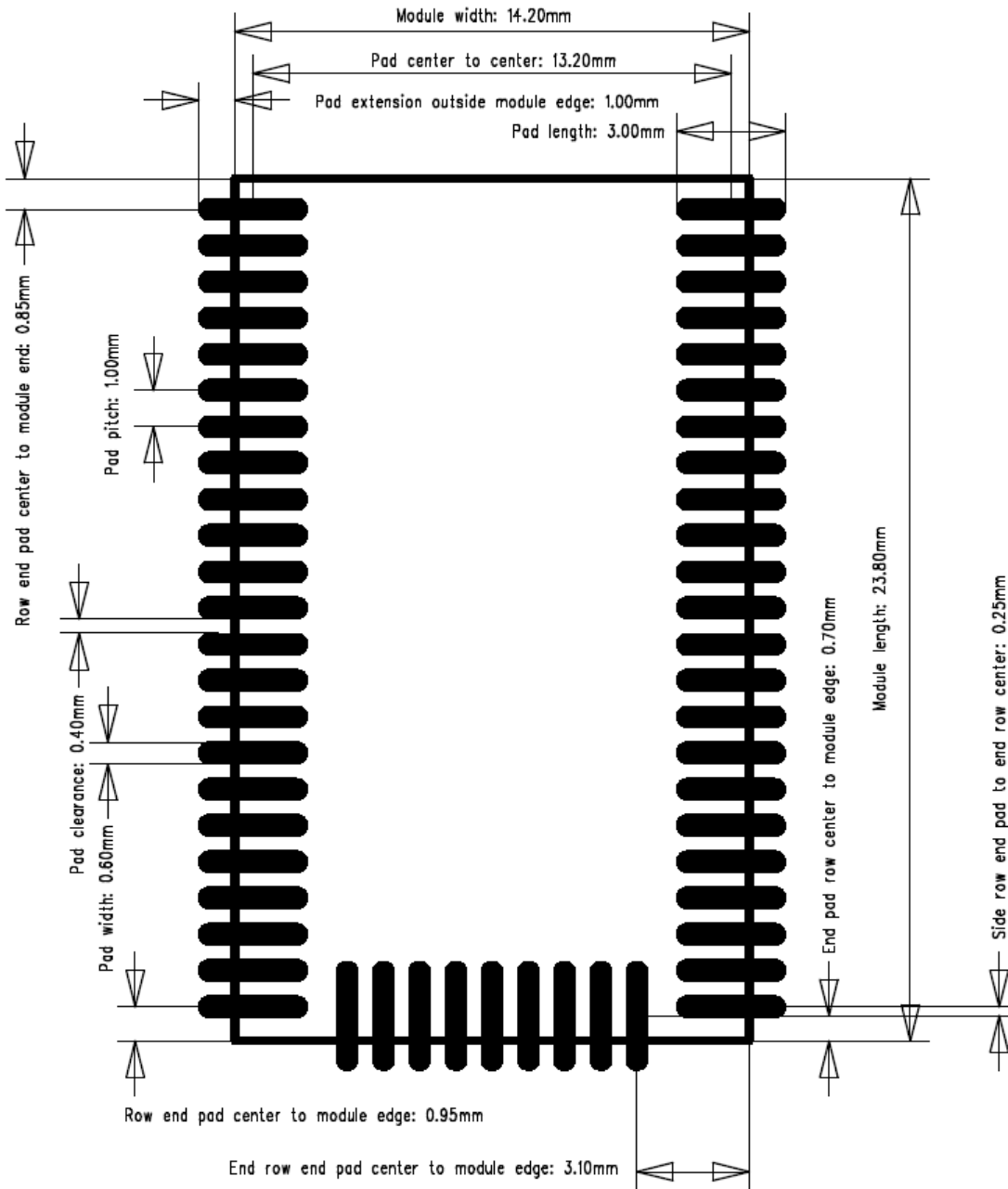
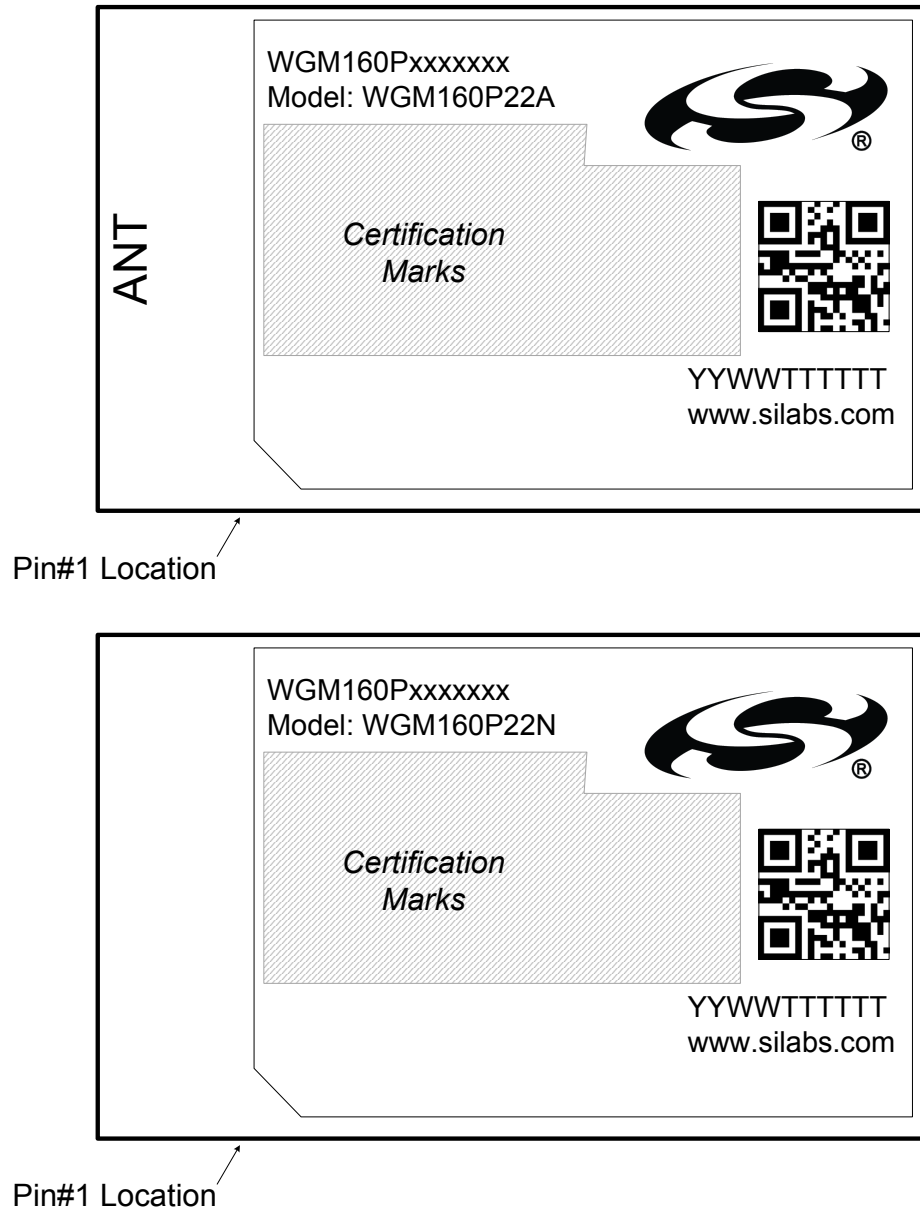


Figure 8.3. WGM160P22N Land Pattern

### 8.3 Package Marking



**Figure 8.4. Package Marking**

The package marking consists of:

- WGM160Pxxxxxx - Part number designation
- Model: WGM160Pxxx - Model number designation
- Certification Marks - All certification marks will be printed in this area according to regulatory body requirements.
- QR Code: YYWMMMMABCDE
  - YY – Last two digits of the assembly year.
  - WW – Two-digit workweek when the device was assembled.
  - MMABCDE – Silicon Labs unit code
- YYWWTTTTTTT
  - YY – Last two digits of the assembly year.
  - WW – Two-digit workweek when the device was assembled.
  - TTTTTT – Manufacturing trace code. The first letter is the device revision.

## 9. Soldering Recommendations

It is recommended that final PCB assembly of this product follows the industry standard as identified by the Institute for Printed Circuits (IPC). This product is assembled in compliance with the J-STD-001 requirements and the guidelines of IPC-AJ-820. Surface mounting of this product by the end user is recommended to follow IPC-A-610 to meet or exceed class 2 requirements.

### **CLASS 1 General Electronic Products**

Includes products suitable for applications where the major requirement is function of the completed assembly.

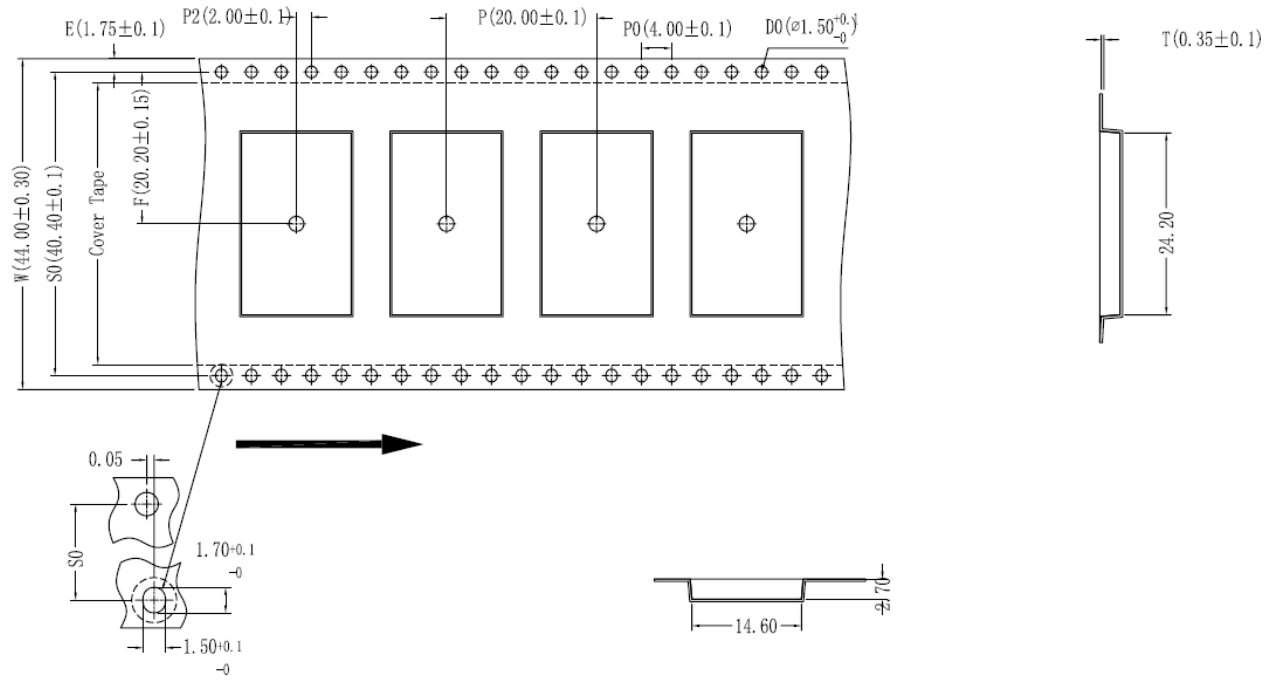
### **CLASS 2 Dedicated Service Electronic Products**

Includes products where continued performance and extended life is required, and for which uninterrupted service is desired but not critical. Typically the end-use environment would not cause failures.

### **CLASS 3 High Performance/Harsh Environment Electronic Products**

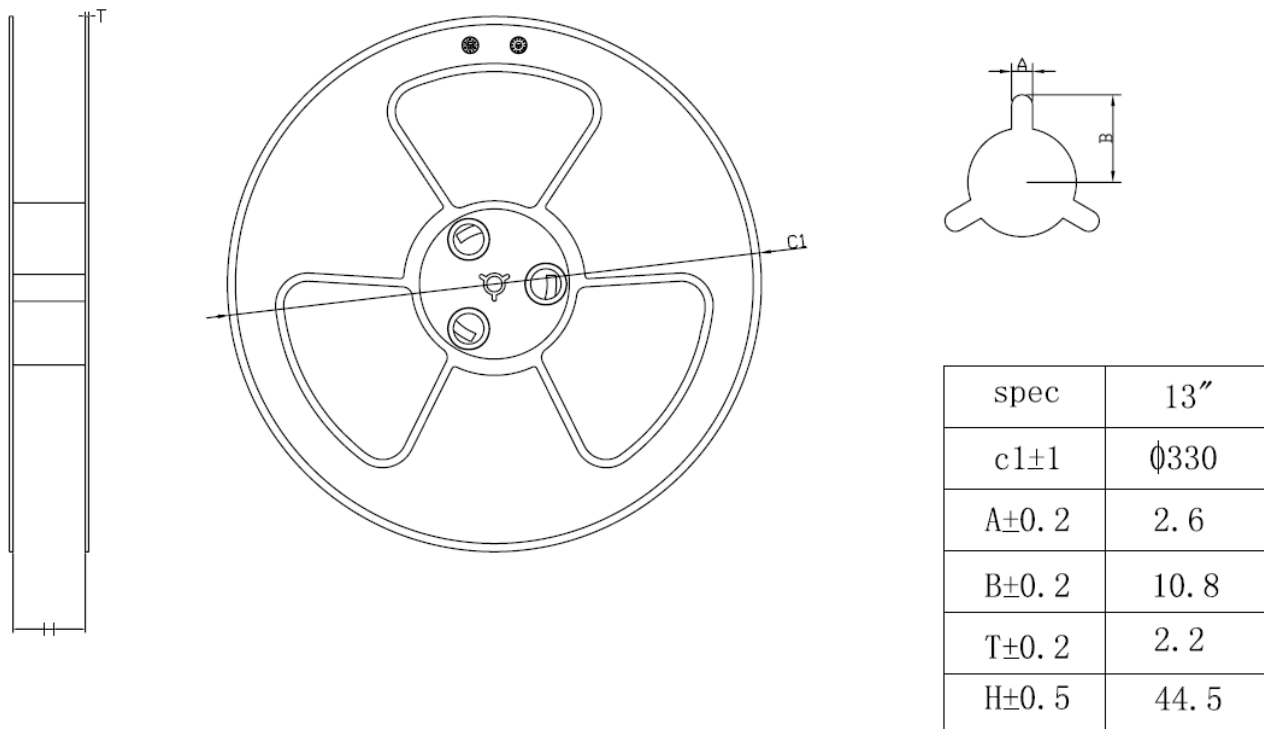
Includes products where continued high performance or performance-on-demand is critical, equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment must function when required, such as life support or other critical systems.

## 10. Tape and Reel Dimensions



All dimensions in mm unless otherwise indicated.

**Figure 10.1. Carrier Tape Dimensions**



All dimensions in mm unless otherwise indicated.

**Figure 10.2. Reel Dimensions**

## 11. Certifications

This section details certification status of the module in various regions.

The address for the module manufacturer and certification applicant is:

SILICON LABORATORIES FINLAND OY  
Alberga Business Park, Bertel Jungin aukio 3,  
02600 Espoo, Finland

### 11.1 Qualified External Antenna Types

This device has been certified with an integrated chip antenna as well as external antennas connected to either RF port or both. The required antenna impedance is 50  $\Omega$ .

**Table 11.1. Qualified Antennas for WGM160P**

| Antenna Type                 | Maximum Gain |
|------------------------------|--------------|
| Connectorized Coaxial Dipole | 2.14 dBi     |

Any antenna of the same general type and of equal or less directional gain as listed in the above table can be used in the regulatory areas that have a full modular radio approval (USA, Canada, Korea, Japan) as long as spot-check testing is performed to verify that no performance changes compromising compliance have been introduced. In countries applying the ETSI standards, like the EU countries, the radiated emissions are always tested with the end-product and the antenna type is not critical, but antennas with higher gain may violate some of the regulatory limits.

If an antenna of a different type (such as a chip antenna, a PCB trace antenna or a patch) with a gain less than or equal to 2.14 dBi is needed, it can be added as a permissive change, requiring some radiated emission testing. Antenna types with more gain than 2.14 dBi may require a fully new certification. Since the exact permissive change procedure is chosen on a case by case basis, please consult your test house, for example while performing with them the EMC testing of the end-product.

### 11.2 CE and UKCA - EU and UK

The WGM160P22A and WGM160P22N modules have been tested against the relevant harmonized/designated standards and are in conformity with the essential requirements and other relevant requirements of the Radio Equipment Directive (RED) (2014/53/EU) and of the Radio Equipment Regulations (RER) (S.I. 2017/1206).

Please notice that every end-product integrating a WGM160P22A or WGM160P22N module will need to perform the radio EMC tests on the whole assembly, according to the ETSI 301 489-x relevant standards.

Furthermore, it is ultimately the responsibility of the manufacturer to ensure the compliance of the end-product as a whole. The specific product assembly is likely to have an impact to RF radiated characteristics, when compared to the bare module. Hence, manufacturers should carefully consider RF radiated testing with the final product assembly, especially taking into account the gain of the external antenna if any, and the possible deviations in the PSD, EIRP and spurious emissions measurements, as defined in the ETSI 300 328 standard.

The modules are entitled to carry the CE and UKCA Marks, and a formal Declaration of Conformity (DoC) is available at the product web page which is reachable starting from <https://www.silabs.com/>.

### 11.3 FCC - USA

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesirable operation.

Any changes or modifications not expressly approved by Silicon Labs could void the user's authority to operate the equipment.

#### **FCC RF Radiation Exposure Statement:**

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End users must follow the specific operating instructions for satisfying RF exposure compliance. This transmitter meets both portable and mobile requirements in accordance to the limits exposed in the RF Exposure Analysis. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter product procedures.

#### **OEM Responsibilities to comply with FCC Regulations:**

OEM integrator is responsible for testing their end-product for any additional compliance requirements needed with this module installed (for example, digital device emissions, PC peripheral requirements, etc.). Additionally, investigative measurements and spot checking are strongly recommended to verify that the full system compliance is maintained when the module is integrated, in accordance to the "Host Product Testing Guidance" in FCC's KDB 996369 D04 Module Integration Guide V01.

- In the typical case when the integral antenna of the WGM160P22A is used, a minimum separation distance of 40 mm must be maintained at all times between the human body and the radiator (antenna) to meet the SAR exemption for portable conditions. When the WGM160P22N is used instead, the minimum separation distance is also 40 mm, unless only the RF port 2 is used with a dipole antenna, in which case the minimum distance is 37 mm.
- The transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter product procedures.

#### **Important Note:**

In the event that these conditions cannot be met, then for the FCC authorization to remain valid the final product will have to undergo additional testing to evaluate the RF exposure, and a permissive change will have to be applied with the help of the customer's own Telecommunication Certification Body.

#### **End Product Labeling**

The variants of WGM160P Modules are labeled with their own FCC ID. If the FCC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. In that case, the final end product must be labeled in a visible area with the following:

**"Contains Transmitter Module FCC ID: QOQWGM160P"**

Or

**"Contains FCC ID: QOQWGM160P"**

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end product.

#### **Class B Device Notice**

**Note:** This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help

## 11.4 ISED - Canada

### ISED

This radio transmitter (IC: 5123A-WGM160P) has been approved by *Innovation, Science and Economic Development Canada (ISED Canada, formerly Industry Canada)* to operate with the antenna types listed above, with the maximum permissible gain indicated. Antenna types not included in this list, having a gain greater than the maximum gain listed, are strictly prohibited for use with this device.

This device complies with ISED's license-exempt RSS standards. Operation is subject to the following two conditions:

1. This device may not cause interference; and
2. This device must accept any interference, including interference that may cause undesired operation of the device

### RF Exposure Statement

Exemption from routine SAR evaluation limits are given in RSS-102 Issue 5.

The models WGM160P22A and WGM160P22N meet the given exemption requirements when the minimum separation distance between the antenna(s) and the human body is respectively 30 mm and 40 mm. In the case of the N variant, the minimum separation distance could also be 30 mm but only in the case of using exclusively the dipole antenna at RF port 2, without configuring any transmission out of RF port 1.

In other words, RF exposure or SAR evaluation is not required when the separation distance is same or more than stated above. If the separation distance is less than stated above the OEM integrator is responsible for evaluating the SAR when using the module at its highest transmission power.

### OEM Responsibilities to comply with IC Regulations

The WGM160P modules have been certified for integration into products only by OEM integrators under the following conditions:

- The antenna(s) must be installed such that a minimum separation distance as stated above is maintained between the radiator (antenna) and all persons at all times.
- The transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter.

As long as the two conditions above are met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

### IMPORTANT NOTE

In the event that these conditions cannot be met, then for the ISED authorization to remain valid the final product will have to undergo additional testing to evaluate the RF exposure, and a permissive change will have to be applied with the help of the customer's own Telecommunication Certification Body.

### End Product Labeling

The WGM160P module is labeled with its own ISED ID. If the ISED ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. In that case, the final end product must be labeled in a visible area with the following:

**“Contains Transmitter Module IC: 5123A-WGM160P ”**

or

**“Contains IC: 5123A-WGM160P”**

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end product.

### CAN ICES-003 (B)

This Class B digital apparatus complies with Canadian ICES-003.



## ISED (Français)

ISED a approuvé l'utilisation de cet émetteur radio (IC: 5123A-WGM160P) en conjonction avec des antennes de type dipolaire à 2.14dBi ou de son antenne intégrée. L'utilisation de tout autre type d'antenne avec ce composant est proscrite.

Ce composant est conforme aux normes RSS, exonérées de licence d'ISED. Son mode de fonctionnement est soumis aux deux conditions suivantes:

1. Ce composant ne doit pas générer d'interférences.
2. Ce composant doit pouvoir être soumis à tout type de perturbation y compris celle pouvant nuire à son bon fonctionnement.

### Déclaration d'exposition RF

L'exemption tirée des limites courantes d'évaluation DAS est donnée dans le document RSS-102 Issue 5.

Les modèles WGM160P22A et WGM160P22N respectent les exigences d'exemption prévues lorsque la distance de séparation minimale entre le(s) antenne(s) et le corps humain est respectivement de 30 mm et 40 mm. Dans le cas de la variante N, la distance minimale de séparation pourrait également être de 30 mm, mais uniquement dans le cas d'une utilisation exclusive de l'antenne dipôle sur le port RF 2, sans configurer de transmission sur le port RF 1.

La déclaration d'exposition RF ou l'évaluation DAS n'est pas nécessaire lorsque la distance de séparation est identique ou supérieure à celle indiquée ci-dessus. Si la distance de séparation est inférieure à celle mentionnées plus haut, il incombe à l'intégrateur OEM de procéder à une évaluation DAS.

### Responsabilités des OEM pour une mise en conformité avec le Règlement du Circuit Intégré

Le module WGM160P a été approuvé pour l'intégration dans des produits finaux exclusivement réalisés par des OEM sous les conditions suivantes:

- L'antenne (s) doit être installée de sorte qu'une distance de séparation minimale indiquée ci-dessus soit maintenue entre le radiateur (antenne) et toutes les personnes avoisinante, ce à tout moment.
- Le module émetteur ne doit pas être localisé ou fonctionner avec une autre antenne ou un autre transmetteur que celle indiquée plus haut.

Tant que les deux conditions ci-dessus sont respectées, il n'est pas nécessaire de tester ce transmetteur de façon plus poussée. Cependant, il incombe à l'intégrateur OEM de s'assurer de la bonne conformité du produit fini avec les autres normes auxquelles il pourrait être soumis de fait de l'utilisation de ce module (par exemple, les émissions des périphériques numériques, les exigences de périphériques PC, etc.).

### REMARQUE IMPORTANTE

Dans le cas où ces conditions ne peuvent être satisfaites (pour certaines configurations ou co-implantation avec un autre émetteur), l'autorisation ISED n'est plus considérée comme valide et le numéro d'identification ID IC ne peut pas être apposé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera responsable de la réévaluation du produit final (y compris le transmetteur) et de l'obtention d'une autorisation ISED distincte.

### Étiquetage des produits finis

Les modules WGM160P sont étiquetés avec leur propre ID ISED. Si l'ID ISED n'est pas visible lorsque le module est intégré au sein d'un autre produit, cet autre produit dans lequel le module est installé devra porter une étiquette faisant apparaître la référence du module intégré. Dans un tel cas, sur le produit final doit se trouver une étiquette aisément lisible sur laquelle figurent les informations suivantes:

**“Contient le module transmetteur IC: 5123A-WGM160P ”**

ou

**“Contient le circuit IC: 5123A-WGM160P”**

L'intégrateur OEM doit être conscient qu'il ne doit pas fournir, dans le manuel d'utilisation, d'informations relatives à la façon d'installer ou de d'enlever ce module RF ainsi que sur la procédure à suivre pour modifier les paramètres liés à la radio.

## 11.5 Locating the Module Close to Human Body

When using the module in an application where the radio is located close to human body, the human RF exposure must be evaluated. FCC, ISED, and CE all have different standards for evaluating the RF exposure, and because of this, each standard will require a different minimum separation distance between the module and human body. Certification of WGM160P allows for the minimum separation distances detailed in [Table 11.2 Minimum Separation Distances for SAR Evaluation Exemption on page 42](#) in portable use cases (less than 20 cm from human body). The module is approved for the mobile use case (more than 20 cm) without any need for RF exposure evaluation.

**Table 11.2. Minimum Separation Distances for SAR Evaluation Exemption**

| Certification | WGM160P with integrated antenna  | WGM160P with external reference dipole antenna            |
|---------------|--|---|
| FCC           | 40 mm  | 40 mm (or 37 mm when transmitting only over RF port 2)    |
| ISED          | 30 mm  | 40 mm (or 30 mm mm when transmitting only over RF port 2) |
| CE            | The RF exposure must always be evaluated using the end-product when transmitting with power levels higher than 20 mW = 13 dBm. |   |

For FCC and ISED, using the module in end products where the separation distance is smaller than those listed above is allowed but requires evaluation of the RF exposure in the final assembly and applying for a *Class 2 Permissive Change* or *Change of ID* to be applied to the existing FCC/ISED approvals of the module. For CE, RF exposure must be evaluated using the end-product in all cases.

**Note:** Placing the module in touch or very close to the human body will have a negative impact on the efficiency of the antenna thus reducing range.

## 11.6 MIC - Japan

The WGM160P22A and WGM160P22N are certified in Japan with number 005-102265 and 005-102264 respectively.

Since September 1, 2014 it is allowed (and highly recommended) that a manufacturer who integrates a radio module in their host equipment can place the certification mark and certification number (the same marking/number as depicted on the label of the radio module) on the outside of the host equipment. The certification mark and certification number must be placed close to the text in the Japanese language which is provided below. This change in the Radio Law has been made in order to enable users of the combination of host and radio module to verify if they are actually using a radio device which is approved for use in Japan.

Certification Text to be Placed on the Outside Surface of the Host Equipment:

当該機器には電波法に基づく、技術基準適合証明等を受けた特定無線設備を装着している。

### Translation of the text:

"This equipment contains specified radio equipment that has been certified to the Technical Regulation Conformity Certification under the Radio Law."

The "Giteki" marking shown in the figure below must be affixed to an easily noticeable section of the specified radio equipment. Note that additional information may be required if the device is also subject to a telecom approval.

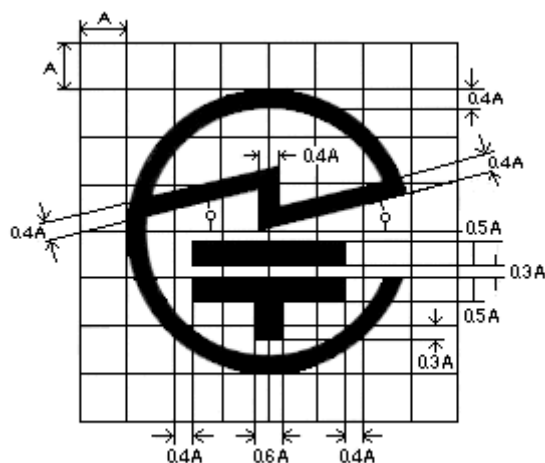


Figure 11.1. GITEKI Mark

## 11.7 KC - South Korea

The WGM160P22A and WGM160P22N are certified in South Korea with number R-C-BGT-WGM160P.

## 12. Revision History

### Revision 1.3

August 2022

- Removed references to Gecko OS from the following:
  - Front page
  - Ordering Information table notes
  - Section [3.1 Introduction](#)
  - Section [7.2 GPIO Functionality](#)
- Updated Section [2. Ordering Information](#) by adding table for revision 4 parts.

### Revision 1.2

December 2021

- Updated Certifications to take into account UK specifics (Section [1. Key Features](#) and Section [11.2 CE and UKCA - EU and UK](#))
- Removed Gecko OS as a software option (Section [4.8 Microcontroller Peripherals](#) and Section [6. Software](#))

### Revision 1.1

September 2020

- Updated [Table 2.1 Ordering Information for Revision 3 Parts](#)
- Updated [Figure 5.1 Example Schematic for NCP Application on page 14](#)
- Updated Chapter [6. Software](#)

### Revision 1.0

March 2020

- Removed WiFi Alliance from certifications listed in Front Page and Key Features
- Added note to [Table 3.1 Supported Wi-Fi Modulations, BW, and Channels on page 6](#)
- Added DTIM and sleep current values to [Table 4.3 Power Consumption on page 8](#) and updated Typical standby current from 638 nA to 217 nA
- Updated Max  $V_{OL}$  from 20 to 25 % and Min  $V_{OH}$  from 80 to 75% in [4.4 Digital I/O Specifications](#)
- Added note about peripherals supported by Gecko OS in [4.8 Microcontroller Peripherals](#)
- Added reference to AN1224 in [5.2 Multi-Protocol Coexistence](#)
- Corrected pin 40 naming from VUSB to VSUB in [Figure 5.1](#)
- Added [11.6 MIC - Japan](#) and [11.7 KC - South Korea](#) certifications

### Revision 0.5

April 2019

- Updated naming for Sections [7.2 GPIO Functionality](#) and [7.3 Alternate Pin Functionality](#)
- Removed TBD Idle currents from [Table 4.3 Power Consumption on page 8](#) and changed term "Sleep" to "Standby"
- Updated [Table 4.4 Digital I/O Specifications on page 9](#)
- Updated [Table 4.6 RF Receiver Characteristics on page 11](#)
- Updated min PCBx\_mm to 40 mm in [Table 4.7 Radiated Characteristics on page 11](#)
- Updated Section [9. Soldering Recommendations](#)
- Updated module manufacturer address in Section [11. Certifications](#)
- Updated text in Sections [11.1 Qualified External Antenna Types](#), [11.3 FCC - USA](#), [11.4 ISED - Canada](#), and [11.5 Locating the Module Close to Human Body](#)
- Updated [Table 11.2 Minimum Separation Distances for SAR Evaluation Exemption on page 42](#)

**Revision 0.3**

Feb 2019

- Updated top-level device details throughout document.
- Removed software details from Section [1. Key Features](#) (moved to Section ).
- Updated Section [2. Ordering Information](#) to expand all OPN details.
- Corrected details in Section [Figure 3.1 WGM160P Block Diagram on page 6](#).
- Updated all tables in Section [4. Electrical Specifications](#) with latest nomenclature and characterization data.
- Added Section [5.3 Example Schematic](#).
- Added Section .
- Updated pinout details in Section [7. Pin Descriptions](#).
- Removed functions not pinned out from Section [7.2 GPIO Functionality](#) and [7.3 Alternate Pin Functionality](#).
- Updated Section [8. Package Specifications](#) with additional landing diagram and package marking details.
- Added Section [9. Soldering Recommendations](#).
- Added Section [10. Tape and Reel Dimensions](#).
- Added Section [11. Certifications](#).

**Revision 0.2**

November 2018

- Initial release.

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